ELFNET Roadmap

European Electronics Interconnection

Version 1

February 2007

INTRODUCTION

Electronic interconnection technologies are in every sense key to global communication, security, safety and quality of life. The major systems and tools that modern society has come to rely on depend on transmission of electric current through joint interfaces.

These technologies are currently undergoing a global revolution with the implementation of new environmental technologies based on removal of hazardous substances from materials used in electronic and electrical equipment under the EU RoHS Directive and other similar legislation targeted for 2006-2010. Continued research and technology development will be vital to responding to this challenge.

At the same time technology drivers are applying pressure to adapt interconnection materials technologies to ever smaller products with greater functionality and a more transparent and efficient life cycle. Some of these trends are quantified in Annex 1.

ELFNET, representing the critical mass of Europe's soldering technology experts, has been working during the transition to lead-free soldering to draw together this community in a series of meetings and web communications to define and resolve implementation issues.

Coherent collaboration in development and implementation of new technologies across European boundaries is the key to ensuring global competitiveness in the face of strong challenges from the US, Japan and the Far East.

This document represents a collective effort to look forward through and beyond the lead-free transition to technological development of electronic interconnection technologies generally. It complements the larger industry-standard documents such as the IPC, iNEMI and ITRS roadmaps, giving a particular perspective on cost-effective, sustainable and reliable technologies.

ELFNET (European Lead Free soldering NETwork) is a European network of national research organisations, technical experts and industry bodies enabling lead-free solutions in micro-electronics. It provides a platform to coordinate, integrate and optimise research, enabling electronic producers in the EU to optimise solutions and meet the EU deadline of introducing lead-free soldering in consumer products by July 2006.

ELFNET is supported by the European Commission and operates in 19 European countries. By facilitating 'best practice', ELFNET will continue to contribute to Europe's competitiveness in electronics manufacturing beyond 2006.

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Supply Chain Management

1. Introduction

Environmental Supply Chain Management (ESCM) has been growing in importance over the last decade across industry sectors. However, only recently has it been driven by urgent legislative and market forces demanding more accountability and reporting on the environmental status of products.

This has been complicated by the trends towards complex, global, networked supply chains. Increasingly the OEM is further and further away from suppliers, both physically and in terms of data exchange. Even product design can now be the responsibility of the CEM.

The electronics industry is a classic example, with very significant increases in out-sourcing of work to CEM's and rapid advances in global procurement, exploiting important opportunities for economy in Central Europe, India and China, for example. Further, Europe has an industry that in some sectors is supported by countless SME's in 25 culturally diverse member states.

The introduction of the RoHS Directive in particular has massively increased the demand for ESCM, both in terms of the need to transfer data on hazardous substances and of the need to cost-effectively source RoHS-compatible components.

Within this new paradigm there is an urgent need to collaborate in achieving harmonisation on information exchange protocols and formats, to avoid a chaotic multiplicity of practices and mountains of paperwork for those responsible for ESCM.

Whilst Japan and the US are largely achieving this, fragmentation and lack of communication has so far meant almost complete failure in Europe.

Looking forward over the next decade, it is inevitable that accepted practices will be developed by evolutionary default in the light of experience, particularly as enforcement regimes begin to have an impact. Further EU legislation, notably REACH, will add pressure shortly.

2. Materials Declaration

Declaration of materials used in supplied components has for some time been an established requirement for suppliers to some OEM's, notably within the automotive industry. Companies such as Ford and Sony use such mechanisms to proscribe and enforce their own environmental policies based on limitation or elimination of substances perceived as undesirable. New EU legislation such as RoHS and REACH are forcing the pace.

The first to address this issue significantly in relation to 'green electronics' was the Nordic GreenPack project 1999-2002. A free web-based tool was produced. The Danish RoHS Implementation Group also now publish templates for declaration.

In 2003/4 a global initiative involving EIA (US), EICTA (Europe) and JGPSSI (Japan) published the Joint Industry Guide (JIG), for generic use, covering what substances need to be reported and basic guidelines on data formats and applicability.

EIA/JEDEC worked with an industry drafting group, including some major European OEM's, to convert this to a standard JIG-101, published in May 2005.

The original JIG began a major revision process in September 2006.

In the meantime, JGPSSI in Japan produced a 'Survey Response' tool and US industry groups delivered IPC standards IPC 1752, with a handbook IPC 1065, both based on the JIG.

A number of other tools are being offered by industry on a more commercial basis, notably in the US. Examples include RosettaNet, GoodBye Chain Group and Omnify Software.

By contrast, the situation in Europe is still rather confused.

ZVEI, alongside EICTA a recognised European trade representative, produced a White Paper on the issue in October 2004 and held a special meeting on the topic in January 2006. This approach was hindered by a lack of clarity from the EU Commission on the precise definition of 'lead-free', with some false expectations amongst some during 2005 that it could refer to impurity levels of 0.1% of a 'unit', the unit being the whole component or even assembly. Thus generic 'Umbrella Specifications' and 'Flat Bill of Materials' were proposed, as used in other materials declaration contexts. It wasn't until August 2005 that the definition '0.1% of homogeneous material' was formally adopted, rendering these approaches inadequate.

The same issue affected drafting of a global standard. IEC TC3 published IEC 61906/DIN 19220 in June 2005. This also failed to 'drill down' to the level of 'homogenous material' required for RoHS compliance. The task to produce a refined standard was passed to IEC TC 111 / HWG 2 but this has become bogged down in competing proposals from the US, France, Finland and even China.

Even now the debate is continuing on what exactly is required for compliance with RoHS. There is no regulation on the topic within the RoHS Directive itself. The current official Commission FAQ refers enquirers to the member state authorities who are 'currently discussing possible approaches'.

The UK's NWML has issued guidelines recommending Due Diligence including 'reasonable endeavours', but is the only member state to officially state this more low-key approach.

EICTA and ZVEI argued for a balanced approach, whereby full declarations are only required in cases where there is reason for concern. Further they were keen to utilise existing quality processes and supplier agreements to increase trust and minimise additional paperwork.

The best available information on what will be required is a non-legally binding guidance document published in May 2006 by the informal inter-governmental RoHS Enforcement Network, attempting to harmonise their enforcement approach.

This makes a distinction between larger companies whose entire product assurance systems will be probed and SME's for whom only product specific documentation will be required, including conformance certificates and RoHS-element materials declarations. All data is expected to be supported by evidence of data quality assessment procedures, including test analysis reports.

What is happening in practice today is hard to assess. Certainly most SME's at least would consider the costs of collating materials declarations for each component/product prohibitive and many are not actively looking at this option. Instead they are just using simple conformance certification (COC) documents covering the whole delivered package, often with wording agreed on a case-by-case basis with customers. Most simply use the BOM to go through the components, gathering whatever data is available from the various suppliers to verify compliance. Some may be unaware that this is not a 'materials declaration' as such. Testing each homogeneous material is also thought unrealistic and testhouses are using an 'intelligent' experience-based approach to sample high-risk components. It has also been deduced that enforcement authorities will initially target a few larger, high-risk producers, allowing mainstream and smaller companies a significant time cushion.

Some OEM's are, however, insisting on materials declarations, notably in the automotive sector.

In fact it is very hard in law to define reasonable measures that a company should take in seeking to comply with such legislation and ultimately clarity can only truly come when test cases have been through the courts.

As a further issue, the actual data on substance content is often in fact not known or trustworthy.

Early efforts to survey suppliers for such data proved massively resource-intensive and singularly unsuccessful in eliciting response. Suppliers have also been slow to release such detailed information on component composition in product datasheets and/or the web. In this regard large component distributors, who sit in the middle of the supply chain, have played a very significant role in collating and publishing such data. Examples are FarnellinOne, and PartMiner.

The pressure to comply will inevitably lead to misrepresentation. Ultimately such data can only be verified by testing. However these protocols are not fully developed either.

The RoHS Enforcement Guidance document does partially address protocols for RoHS testing including sampling, following the generally accepted approach of XRF screening, with by more detailed tests as required. However, reference standards for relevant laboratory tests are still under development and a draft IEC standard from TC 111 / WG3 on Test Methods is in draft but not yet released.

Surveying this situation and looking into the future it seems clear that in the short-term there will exist a gap between currently stated theoretical compliance requirements and actual practice.

Companies are being forced by this paradigm shift towards implementation of a form of ESCM, though how this will involve materials declarations in not entirely clear. Given the considerable industry resistance and inexperience, coupled with a lack of clear guidance and leadership in Europe it could take maybe 5 years or more before industry practices are harmonised at an adequate level.

It is important to the competitiveness of the European market that variation in enforcement practices between member states is minimised. The continued work of the RoHS Enforcement Network will be important in clarifying what is required and this will need to be illustrated by test cases in court. National agencies need to do more to disseminate the available guidance, to SME's in particular, utilising available industry information agencies and networks.

European trade associations, by contrast with US and Japan, have not been able to provide positive leadership and, once it is confirmed that materials declarations are indeed required, need to address this issue on behalf of the industry.

The IPC-1752 standard does exist, along with implementation tools and is being used by European companies. However the rigours of such a protocol are a strong deterrent.

The IEC standards process has shown a number of critical weaknesses, with delays, conflicting proposals and a lack of knowledge of what exactly is required. It is not clear today whether an IEC standard will ever be produced.

Technical and standards work on RoHS testing is underway by competent parties but needs completing with a high priority. Important developments in RoHS testing are expected in the next year.

In the longer term a technological solution can be foreseen whereby materials data is included in data sets exchanged within advanced supply chain IT communication systems. The demand for such systems is likely to grow as supply chains continue to become more complex and manufacturing becomes more virtual. For example, embedding of data in RFID tags within components could be envisaged.

There is, however, a large technology gap between such a system and today's PC/paper-based protocols, many using basic tools such as Microsoft Excel, Word and Adobe Acrobat. There is also an issue with the multiple IT platforms used, some highly customised and many very capital intensive. The iNEMI Materials Composition Data Exchange project, associated with the development of IPC 1752, made significant advances in moving towards universal data exchange formats.

3. Marking & Labelling

Lead-Free Labelling

It was assumed in the early development stages of lead-free soldering that some form of labelling would be used to denote products and components that were lead-free soldered. In practice this has proved a more complex challenge.

The initial focus was on a 'lead-free' symbol – for example a leaf or crossed Pb symbol. Panasonic used a leaf symbol on their Minidisc player when it was released in 1999. European contributions to this field came from Soldertec and from the EFSOT project.

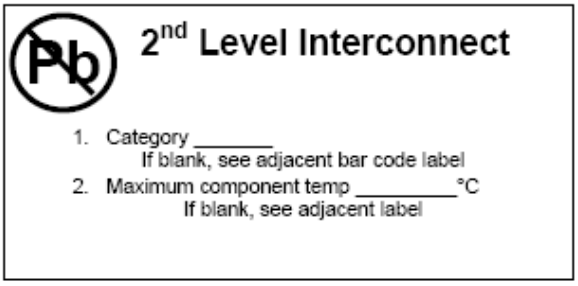
Multiple variations of such symbols began to propagate and the debate broadened as industry began looking for a 'RoHS-compliant' label rather than just 'lead-free'. Over time it was perceived that the purpose of many such symbols was mainly marketing, although they are useful on packaging for customs and inventory control. Both the IPC and IEC refused to consider a compliancy-based standard.

Compliance markings have however developed through various quality assurance agencies, as a part of their normal operations. Examples are the BSI 'RoHS-Trusted Kitemark' and the TUV 'RoHS Mark'.

Technical efforts have since focussed more on using a marking to convey useful technical materials information to assist with compatibility issues in assembly and upstream work such as rework, repair and recycling.

In 2004 JEDEC published JESD97 and IPC published a new version of IPC-1066. These have now been combined and will be republished as J-STD 609 shortly.

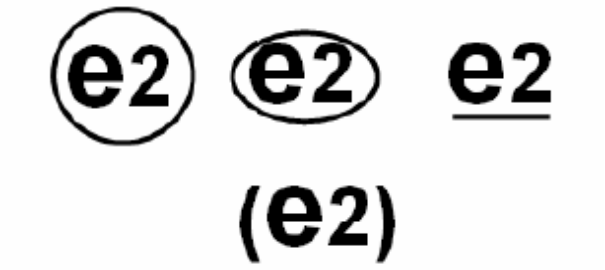
These standards focus on 2nd Level Interconnects, defined as the connection made be attaching a component to a circuit board. They provide labels for components with simple crossed-Pb symbol, Category and Maximum components temperature.



J-STD 609 Component label

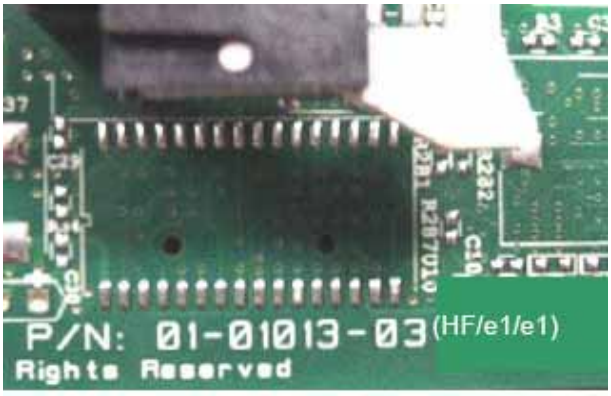
Categories define the material/terminal finish, for example 'e2' is SAC alloy.

Board level markings are also included in



J-STD 609 Material category label examples

the J-STD 609 standard, with a standardised code sequence. This includes 'HF' (Halogen-Free), 'eX' codes for solder and finish, 'bX' codes for board finish and 2 letter 'XX' codes for conformal coating.



J-STD Board marking example

One weakness of this approach is that some components are far too small for any kind of marking. There are obvious problems with bare die, for example. In this case the marking can only be used on the lowest level shipping container.

In 2004 the Japanese produced a Guidance Document ETR-7021 and a report on semiconductor marking EIAJ EDR-7605. These showed some disharmony with the US approach. For example more detailed coding is used to describe the exact solder alloy composition used. 'A30C5' for example, denotes Sn3Ag0.5Cu alloy. In July 2005 a Guidance Document ET-7001 was published.

Finally a Japanese standard JIS C 950 was published in December 2005. This covered all RoHS elements and introduced new symbols:

Japan JIS C 950 markings

These labels are used in conjunction with whole product labels describing the various sub-parts of equipment – speakers, cabinet, CRT etc – and stating whether or not RoHS elements are present in each.

These same symbols, but with different content are also being used in China in a standard currently being drafted.

These markings have a particular significance, because, unlike the RoHS Directive, they will form a part of the legal enforcement of substance bans in Japan and China.

As for a global standard, the IEC TC97 stalled in December 2005 over competing proposals and questions over the feasibility and use of a unified label. It has been decided that instead a Technical Specification will be published, initially based on a Japanese proposal.

Apart from the Japanese approach, current concepts for marking are not comprehensive enough to deal with the total supply chain, recycling, repair, end-of-life treatment etc. Neither do they include information on complexities such as RoHS exemption.

To summarise, the debate over different markings appears to be resolving into identifiably different types of marking.

- Customised packaging-based labels for marketing, customs and inventory control
- Product-based RoHS compliance markings issued by recognised quality agencies
- Product-based RoHS substance declarations by sub-part
- Component and Board-based technical markings

US standardisation processes have focussed on the latter type, for lead-free and halogen-free only, and this has been

followed by those Europeans who are using technical markings. The Japanese and Chinese approaches have additional product-based substance markings and are broader, covering all RoHS elements. The IEC contribution remains to be seen. Other label types are industry driven only.

From a European perspective there is no rationale or available agency to begin any new independent initiatives. In practice the J-STD 609 will probably be adopted for technical marking. Customised product and packaging-based labels are likely to continue in the short-term.

It is probably not too late for an authoritative industry-based European forum to consider the status of marking & labelling and provide clear guidance on appropriate action for companies. Enough information and clarity now exists to enable reasonable forecasting and planning. Such a forum could also collate industry feedback and respond to the request of IEC TC91 committee for input to the proposed Technical Specification.

In the medium-term, once the RoHS transition is complete, perhaps by 2010, the incentive for labelling in general is likely to diminish, since the majority of goods will be RoHS compliant.

In fact it is probable that the focus of attention will turn to labelling non-compliant products, particularly for sectors such as aerospace and defence where obsolescence is a significant issue.

Recycling will grow in importance and requirements, such as those already in the WEEE Directive, to label goods with the presence of hazardous substances may become a major issue. In this case the Japanese substance-declaration approach is most relevant.

Technical markings are likely to persist as their information will continue to be relevant in assembly and repair/rework. It remains to be seen whether new lead-free materials will proliferate or whether the industry aim to move towards single solutions will be achieved. This will to some extent determine the long-term future of this type of marking.

As for Materials Declaration, there could be significant technology advances over the next decade beyond the current paper/package-based labelling systems towards advanced IT-based solutions carrying a larger data set in a more comprehensive, readable and transferable form.

2D bar-coding is an intermediate technology step, but this relies on universal use of barcode reader technologies and, ideally integration with existing inventory systems.

Component Numbering

Whether or not to renumber components as lead-free/RoHS compliant has been a significant debate in practice.

Whilst it may seem logical in regard to the ability to inventory control and separation of complaint and non-compliant components, many component suppliers were reluctant to do so.

Part of the issue relates to how long the RoHS transition is expected to be. In theory, if it is reasonably short then a great deal of extra investment would be required to, for example, add a prefix to each component even though this would become redundant once all components were RoHS-compatible. In fact the situation would the reverse since it would then be necessary to identify the minority of non-compliant products.

Philips, who didn't change numbering, argued that doing so would unnecessarily increase customer's costs in BOM revisions and doubling of inventory control systems. In any case, for the majority of components there were no compatibility issues. In fact many shipped components, passives in particular, were already lead-free for some time without the customer realising.

The majority of users, however, gave very strong positive reactions to surveys in the US demanding that part numbers were changed. The NEDA RoHS Summit in January 2006, for example, concluded with a statement demanding new numbers.

With new part numbers it is more obvious when the transition had been made for each component, instead of relying on individual date-based change information. This enables segregation and reduces the risk of cross-contaminations. The case is particularly strong for BGA's where there is a higher risk of compatibility problems and very significant cost of failure should a lead-free product be used unknowingly in a SnPb process. The aerospace/defence industries have particular needs, including the simplest possible way to track non-RoHS components for obsolescence processes.

In response, some component distributors chose to renumber parts themselves. FarnellInOne is an example. Another distributor, Arrow, launched an online database of suppliers marking and numbering policies.

For some companies, relocating incoming parts and product designs into a fully-segregated system, the renumbering issue becomes largely irrelevant.

There have been calls for standardisation of practice regarding the new numbering systems used, since there are currently a myriad of different coding systems used by suppliers. However in practice this appears to be rather too late and unrealistic.

Component renumbering example

Thus all has probably been said and done that could be on this issue. The status quo is clearly non-ideal, but hasn't yet been an obstacle to implementation.

As RoHS implementation proceeds during the next decade, systems will continue to adapt as at present. Renumbered components will probably remain so, otherwise disruption will duplicate in the reverse sense. Identification of non-compliant components will become more important for exempted industries such as aerospace/defence.

4. RoHS Component Availability

Availability of RoHS compatible components has always been a high priority concern for the industry. In the early years of the development there was a strong impression that the components suppliers were not responding and indeed, some research work was hindered by lack of components.

However, major suppliers appear to have largely met the July 2006 deadline for relevant product sectors at least. Passive components have in fact been available for some time.

Major component distributors have seen competitive advantage in making available RoHS information, component databases and products and provided a strong link in the supply chain as a result.

Still, there are thermal stability issues with some actives, notably those that are particularly temperature sensitive. Examples are tantalum caps and LED's.

Of major concern to currently exempted sectors is the continued supply of non-compliant SnPb components. These will be required by, for example the aerospace/defence sector for many years to come – not just for manufacture but also to deal with obsolescence. Major procurement operations for SnPb components have been underway for some time.

There is reason for some concern over the continued supply of some SnPb products, with reports that some suppliers will axe up to 1/3 of their inventory due to non-profitability. Over time it is predicted that the cost of SnPb components may rise as supplies become restricted.

It is now clear, however, that dual supply of SnPb and Pb-free products may be needed for some time. SnPb BGA's will be especially required since lead-free products are less compatible with SnPb processes. The lead-free transition period is likely to extend to 2010 and beyond. For example recent recommendations regarding Category 8&9 products have referred to 2016 as a target date for some equipment.

During the transition there is enormous cost pressure for smaller suppliers who failed to clear inventories in time to pass off components as RoHS compatible. Already a grey market has appeared and counterfeiting has been detected. This is a short-term issue.

Recently a new RoHS exemption has been approved for lead in finishes of 'fine-pitch' components, over concerns related to tin whiskers. It may be however that this has come too late to effectively reverse transition to lead-free finishes for such components.

Future work will be needed to complete the development of compatible components, particularly materials technologies for thermally challenged products.

Exempted sectors are already considering supply and obsolescence issues strong enough drivers to make the lead-free transition without direct legislation. However these sectors are generally also concerned about reliability and this will need to be addressed.

Supply Chain Management

High Priority				
Issue	Challenges	R&D Needed	Notes	Target
Materials Declaration	More clarity on what is required	Study of industry practices	Review ZVEI, IPC, JEITA proposals	2010
		Clear, harmonised industry-led guidance with government support	Link to EU RoHS Enforcement Network	2010
	New tools for materials data handling	International standard on materials declaration templates and data formats	IEC standard required – target 50% use by 2010	2010
		New concepts for multiple degrees, levels of declaration with direct relation to RoHS, REACH etc compliance	Refer IPC 1752, 1065	2010
Marking & Labelling	Industry harmonisation	Study of industry practices	Assess use of IPC standards, J-STD-609	2010
	Clearer standards	Better definition for IPC\JEDEC e1-e9 classification, especially e3-tin	Use e0 for SnPb	2010
RoHS Component Availability	Thermally compatible components	New materials, designs for mitigation of thermal damage to components, laminates	Industry to develop guidelines	2010
	Shelf-life data for new components	Comprehensive review of shelf-life issues for lead-free components and laminates including solderability, MSL, processability	Work with COG forum. Propose IEC TC91/WG10 delamination guideline, towards a standard	2010
	Continued availability of SnPb products	Formation of RoHS-exempted industry groups to consider measures relevant to SnPb supply – obsolescence, labelling, mixed assembly, lead contamination, reliability	Work with COG Forum.	2010

Medium Priority				
Issue	Challenges	R&D Needed	Notes	Target
Marking & Labelling	Industry harmonisation	Industry-led guidance	Review and combine IEC, IPC, JEITA. Input to IEC TC91.	2015
	More efficient data transfer	UV labelling on fully compliant components		2015
RoHS Component Availability	Better RoHS Testing	European standardisation of equipment, protocols and calibration for RoHS testing	IEC standard in development (delayed)	2015
		New standards, reference materials for XRF testing		2010
		Certification by independent, accredited European agencies		2015

Low Priority				
Issue	Challenges	R&D Needed	Notes	Target
Marking & Labelling	More efficient data transfer	New product tagging and data tools based on RFID-type technology		2020
		New cross-platform tools and protocols for data exchange		2020
RoHS Component Availability	Thermally compatible components	More thermally efficient soldering process equipment, reducing excess temperature		2020

Modelling & Design

1. Introduction

With the increasing complexity of the modern world there is a generic demand for more modelling and simulation to be used to characterise systems and provide design input, as well as for new design tools. These are required to optimise systems management and reduce costs.

In the case of electronics interconnection this has a strong relevance in a number of ways.

Electronic designs are rapidly becoming smaller with higher interconnection densities and increase in component mix. Design tools and design rules will need to be evolved to better deal with emerging technologies such as embedded systems, 3D interconnects, 3D-MID and mixed mode wireless.

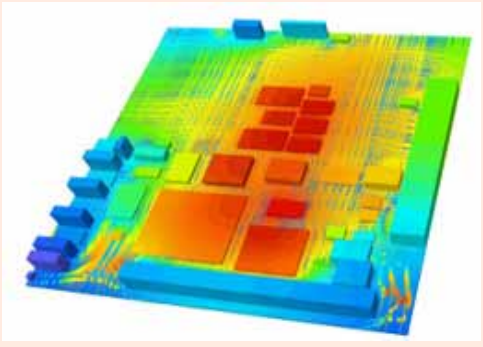
Indeed, there are few if any tools relevant to impending developments in nanoscale, chemical, biological and opto-electronics.

Within mainstream design, new objectives are proliferating to meet demands for optimisation of reliability, manufacturability and environmental compatibility, for example. All of these issues have been recently prioritised by the introduction of lead-free soldering, coupled with significant changes to the electronics supply chain structures.

Lead-free solders with a diversity of sometimes complex microstructures are replacing ‘standard’ SnPb solders. Basic materials data is only just now being compiled to feed solder joint modelling tools, though new models for reliability are only in their infancy.

Thermal issues have become dominant, especially in lead-free solder processing of large and complex boards, with experience of warping, delamination and other effects. New work on modelling is underway to characterise heat and stress distribution, optimising design and mitigating process problems.

Modelling will be used increasingly for simulation of supply chain management, assembly and test procedures.



2. Stress Modelling

Modelling of stress in electronics assemblies and solder joints is an advanced science, using FMEA and other techniques, benefiting from recent improvements in data handling and computation speeds. It is used in design and also to predict product lifetimes.

Europe has many research centres specialised in this area from universities, RTD's and large companies. A sample can be seen in the list of organisers of the EuroSIME group. This group has held annual conferences on thermal, mechanical and multiphysics simulation for a number of years.

The scope of this topic is potentially broad and could include semiconductor packaging, MEMS, flexible circuits and conductive adhesives for example.

The proliferation of new devices and new forms, such as embedded devices will need to be handled by the modelling tools of the future.

However, a focus on lead-free solder joints is the most generic, high impact and urgent approach. The key driver is a link to reliability, where large sectors of the currently RoHS-exempt sectors have concerns. ELFNET has established an expert group for lead-free solder joint reliability whose work could include specific activity on modelling.

However, the impact of lead-free soldering has been so great that an already complex science has required radical rethinking. With regard to lifetime prediction, for example, models for long-term reliability (> 5 years) were not even available for SnPb joints. Now, for lead-free solders, lifetime prediction is "at zero".

The problem is centred on the complexity of the new solder materials. We are moving from a largely simple, single SnPb material to several mutlielement material solutions, with complex microstructures, new properties and new failure modes. Whilst the basic joint geometry remains the same, the materials properties need understanding before models can work. This could take years.

ELFNET has worked with the COST 531 initiative to take a first step in this direction by publishing a comprehensive database of lead-free solder alloy properties, initially listing 32 SAC alloy family members. This is being expanded to other alloy families.

The fundamental micro-nano structural basis for this data is still being explored, with new data on brittle-ductile behaviours, interface morphologies and creep still being produced. What is already known is that much of this is non-linear and inhomogeneous, questioning viability of modelling at this level.

Further, there is a realisation that lead-free solder joint properties can be a function not just of the material but of the component geometry and substrate warpage, for example. This could lead to an alternative and more empirical approach, using a more holistic model of the electronic assembly, with greater consideration of the mission profile and more linkage to real-life field data.

3. Thermal Simulation

Process Modelling

Thermal issues in solder processing have become much more important now that the increased temperatures and narrower process windows of lead-free soldering have to be considered.

This was initially driven by concern over temperature sensitive components particularly, but more recently by issues related to substrate damage for larger and more complex boards.

Here it was realised that problems were not solely a function of solder, component or substrate materials, but also of assembly design. Positioning of larger heat-absorbing components and via density for example can be aggravating factors. Thus a holistic approach may be able to give the most valuable data.

Here, good modelling is clearly desirable as a cost-effective alternative to the trial-and-error approach.

Several new developments are currently in progress aimed at adaptation of traditional software such as Flowtherm for use in process modelling. It is expected that there will be more advances in this area.

Whilst most of the focus may be on mass soldering techniques, and reflow soldering in particular, there is also application to manual soldering, and rework/repair processes in particular, where some severe thermal issues have been observed in some cases.

Joint Modelling

Thermal modelling of electronic interconnections has a number of relevancies and is likely to become more important as the complexity of electronics interconnection technologies increase.

Much work has been done and will continue to be done to study the solidification processes in solder joint formation, particularly in relation to microstructure development. An example is the MICRESS software.

Work is in progress by Prof. Muller at TU Berlin and Prof. Geers at TU Eindhoven.

Modelling is also being applied to development of new soldering techniques such as laser soldering to study localised heat dissipation.

Similar technology is applied along with stress modelling to simulate joint reliability, including thermal cycling tests.

Thermal simulation will become more important for nanoelectronic or embedded interconnections where thermal effects may be important but where tools for practical measurement of such effects are constrained by size or access limitations.

4. Design Tools & Methodologies

The proliferation of new electronic interconnection technologies, both at the PCB and component packaging level, will continue to challenge design tools and methodologies. At the same time, design and the integration of design with assembly processes is likely to become more important in cost-effective systems management.

Adaptation to the new technologies is likely to require very significant investment in tools that are already considered expensive.

There is now a whole family of terms pointing to the growing importance of design including Eco-Design, Design for Environment (DfE), Design for Manufacture (DfM) and Design for Reliability (DfR) for example.

DfM is concerned with creating new ways of optimising the manufacturing operation by, for example thinking more carefully about test access points and equipment limitations. Breakthroughs will come from better business integration between the design and manufacturing functions, often dislocated both geographically and culturally by OEM outsourcing.

In the case of radically new technologies such as lead-free soldering it can be the design function that lags behind and this needs to be addressed by personnel training, better cooperation with experts and a stronger sense of responsibility for the whole product manufacture.

Technology advances will include better tools and algorithms for multi-platform, multi-site data transfer. Assembly feedback systems will improve efficiency.

DfR will become very important for so-called high-reliability applications in harsh environments – automotive, aerospace and defence, for example. However, for lead-free soldering and also other new technologies, the basic principles of reliability and joint failure are as yet missing basic understanding and necessary parameters.

An example of the linking of design with reliability in the field of lead-free soldering is the work of the iNEMI High Reliability Task Force, who are issuing guidelines, including materials selection, for mitigation of tin whisker risk.

5. Standards & Design Rules

Collaborative processes for producing standards and design rules typically suffer from a lack of engagement under normal circumstances but then lack the speed and representation demanded when revolutions such as lead-free soldering are introduced.

Inevitably, especially in a fragmented Europe, there can be a lack of leadership, harmonisation and even technical knowledge. In some specific examples for lead-free standards there have been significant difficulties in achieving global harmonisation. US IPC\JEDEC processes have arguably achieved faster and higher profile progress. Japanese developments have been important but lacking in communication.

Completion of standards revision for lead-free soldering is thus likely to take several years.

Several projects focused on European SME's in particular have produced design and/or workmanship guidelines for lead-free soldering. The first was probably the Scandinavian NoNE project. More recently the EU projects GREENROSE, LEADOUT and LFS-for-SME's have attempted to provide such tools.

There are some specific requirements for harmonisation, in connector designs for example. The wide variety in lead-free finishes has led to some calls for better harmonisation and/or movement towards a single solution.

There are also broader needs for improvement of the basic standards protocols themselves. As technologies become more diverse generic standards may need to be developed into more precise and more sector-specific documents.

High Priority				
Issue	Challenges	R&D Needed	Notes	Target
Stress Modelling	Better collaboration	European expert group	ELFNET reliability network	2010
	Knowledge of interconnection properties	Lead-free solder alloy properties database	Extend ELFNET/COST 531 database. See also SURDAT.	2010
		Tools for modelling of solder alloy microstructure evolution and ageing	Some work in progress	2010
		Effect of solder creep - interaction with stress, material behaviour – cracking, stress relaxation	Needs connection with failure	2010
		Collation and analysis of real-life field data for solder joint behaviour.	Company-specific infrastructure to collect non-public information	2010
	New tools and methodologies	Categorisation of stress missions	Very product specific, but material suppliers need defined standards	2010
Design Tools & Methodologies	Design for Reliability (DfR)	New tools and protocols for high reliability products	Modelling, failure modes	2010
		Inclusion of statistical algorithms	Mathematical models to be converted to statistical software packages	2010
Standards & Design Rules	More harmonisation	Lead-free finishes		2010
	Adaptation to new technologies	New pad designs foe lead-free technology		2010
	Better standards	More precise specifications with more pass/fail criteria		2010
		Sector-relevant approach - high temperature, high reliability, harsh environment, consumer, military etc products	Product-specific tests ideal	2010

Medium Priority				
Issue	Challenges	R&D Needed	Notes	Target
Stress Modelling	Knowledge of interconnection properties	Modelling tools for alloy thermo-physical and mechanical property prediction		2015
		Use of quantum mechanics, atomic level R&D, to better understand nanoscale complexities of interconnections		2020
	New tools and methodologies	New tools for measuring stress/strain in warpage for acceptance criteria		2015
		Non-linear models for new failure modes e.g. brittle, IMC, interface reactions for acceptance criteria		2015
		Use of statistics in structural analysis for Design Rules to analyse maximum dispersion of dimensional parameters	Limits dispersions	2015
Design Tools & Methodologies	Cost	More cost-effective design tools, and methodologies e.g. direct data transfer to assembly		2015
Standards & Design Rules	More harmonisation	Land patterns within package diversity		2015
	Adaptation to new technologies	Complete revision of European standards for implementation of RoHS/lead-free technologies.		2015
		Emerging technologies e.g. embedded devices, 3D interconnection, 3D-MID, plastic electronics		2015
		Better board sub-panelisation for smaller form factors		2015
		Shear-pull tests		2015
		Warpage measurements	Real-world verification	2010
		Microvia definitions		2010

Low Priority				
Issue	Challenges	R&D Needed	Notes	Target
Stress Modelling	Knowledge of interconnection properties	Use of quantum mechanics, atomic level R&D, to better understand nanoscale complexities of interconnections		2020
		Fundamental materials data for nanoscale and biological interconnections		2020
	New tools and methodologies	Holistic FMEA approach integrating influence of materials, process, degradation etc		2020
		Atomic level models for predictive failure on nanoscale		2020
Thermal Simulation	Adaptation of FEM tools to new technologies	New tools for holistic thermal simulation at product, board, component and joint levels in both process and use.		2020
		Scaling of models from board level towards nanoscale interconnection		2020
		Parameters for new materials, including intermetallics		2020
Design Tools & Methodologies	Adaptation of tools to new technologies	Improved tools for emerging technologies e.g. embedded passives, optoelectronics		2020
		Integrated tools for mixed-mode wireless		2020
		New tools for high density designs		2020
	Cost	Simulation of assembly line performance, supply chain management, QC tests for optimum ROI		2020
	Better design for manufacturing (DfM)	Identification of factors, generation of metrics		2020
		Inclusion of test access in design		2020
		New multi-platform, multi-site data transfer protocols.		2020
		Improved DfM algorithms for CAD		2020
		Better systems integration e.g. assembly data feedback, OEM in-house DfM		2020

Materials Technologies

1. Introduction

Never before has the electronics industry faced so many radical changes in the basic materials used for its assemblies. Compatibility issues mean that the advent of lead-free soldering is not only changing the basic solder alloy but also component and board finishes, boards and component packaging materials. Further, the impact of halogen-free legislation has not yet been fully realised.

Work on alternative lead-free solder alloys has been underway since the 1980s and it has taken many years since to study interactions with metal finishes on components and boards and develop new solutions. This work continues and is likely to do so for the foreseeable future.

Research continues to build and refine solder alloy compositions based on the basic SAC alloy family and widen the scope to include low temperature and high reliability solutions. At the same time, the recent industry experience of the high costs and reliability risks of qualifying new solders is pressuring against new variations and towards single solutions.

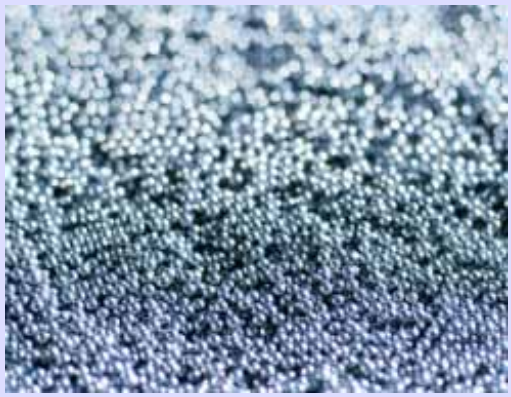
There is still no viable cost-effective alternative to high-lead high temperature solders used in component packaging.

Work on conductive adhesive technology as a replacement for soldering altogether continues but faces significant challenges.

Other assembly materials such as underfills, encapsulants and inks are also being adapted to the new processing environment. Conformal coating technology needs some new thinking.

Substrate technology is not in general dealing well with the twin challenges of higher processing temperatures for lead-free soldering and the need for halogen-free solutions. This needs urgent attention.

Work needs to be done to develop materials with better CTE matching to mitigate current thermal issues in both processing and use.



2. Lead-Free Solders

SnAgCu Solders

The SnAgCu, or SAC, alloy family, with its reduced form SnCu, has become the alloy of choice for the majority of the European market. This recommendation was made by both Soldertec and iNEMI in 2000, following results of earlier projects, notably the IDEALS project in Europe.

They had already been applied in the automotive industry for under-bonnet applications due to their improved robustness over SnPb.

There has been a plethora of formulation variations with the SAC alloy family, with 33 being chronicled in ELFNET/COST 531 database. This has been largely due to patenting and commercial issues. The IPC Solder Products Value Council recently studied the effect of this variation in a large collaborative program and concluded that there was very little performance difference between commonly used formulations.

Low-silver alloys have nevertheless been an important new development, mainly aiming at reducing costs of Ag. Work has included the discovery that SAC101 has benefits for use in BGA solder ball adhesion and shock resistance in mobile devices.

More significant variation is likely to arise from practical effects such as differences in solder alloy paste properties. Most of Europe's major solder manufacturers have been key players in lead-free soldering research since its beginning in around 1990. They have been able to refine solder ball production, size distribution, flux chemistry and paste rheology, for example. A large number of smaller suppliers have needed to catch up with this proprietary knowledge. Thus there have been very wide variations in paste performance for nominally the same alloy formulation and this is likely to continue throughout the lead-free transition.

Solder pastes have been adapted for specialised use, for example tombstoning prevention and voiding control. It is likely that suppliers will continue to compete for differentiation in this way for some time and that paste and flux technologies will evolve over the next few years.

SAC+ variants began to appear quite early in the transition, the most well-known being the Nihon Superior 'Ni-stabilised' product, claiming improved wettability and finish, notably for SnCuNi in wave soldering.

Early projects explored the effects of the additional elements of SAC alloy properties, in particular amongst the automotive community who were seeking to strengthen the alloy. An example was the INNOLOT project. These effects are now reasonably well-known and some results were presented within ELFNET.

SAC alloys with Ni, Co, Mn and Ge are now also used as ball materials for arrays.

However, whilst the effects of these additions on microstructure are known to some degree, the links between microstructure and reliability are only now being explored. Thus this, along with the concept of adding nanoparticles in so-called 'composite solders' can still only be largely empirical.

Nevertheless, with the strong pressure for high-reliability applications to conform to lead-free solutions projects such as the

GEAMCOSS and AMELIE projects aimed at 'high-reliability solders' are likely to multiply and will contribute well to the basic science.

Low Temperature Solders

A major reasoning for introduction of SAC alloy was the tolerance of lead in a transitional period. It was envisaged that second generation alloys, potentially cheaper and lower temperature processing, would later be introduced.

There is also a desire to use lower temperatures to avoid thermal problems from lead-free processing and also to reduce energy consumption.

Much research has already been carried out on SnZn, SnBi, SnZnBi alloys and their myriad derivatives as well as other low temperature solutions. Japan particularly has focussed on this area, since in any case their more eco-efficient soldering equipment allows lower temperature operations.

There are significant technical issues to be overcome, notably the oxidative instability of SnZn both as a solder paste and at joint interfaces. A stable flux is required, but these are likely to be a proprietary technologies rather than amenable to collaborative research.

Many solutions have been devised to overcome these issues for SnZn, notably addition of other elements. There is strong research and commercial interest in Europe to look at this topic more.

Some SnZn solder has been in commercial use in Japan for some years.

However, it appears that both solder manufacturers and CEM's are extremely reluctant in fact to take this route. Claimed benefits in material cost are small compared to the costs now known to be associated with qualifying a new solder alloy for use. Further the benefits of lower temperature are diminishing as materials and equipment is redesigned to adapt to higher lead-free temperature as industry standard.

There are also lingering sustainability doubts in Europe about using Bi, even if the Bi-lead compatibility issue does eventually become redundant.

An entirely different new approach explores the concept that use of nanoscale solder paste particles can be used to decrease melting point. This is discussed further below.

High Temperature Solders

High lead, high temperature solders used inside components for applications such as die attach have been specifically exempted from the RoHS Directive since the consensus is that a cost-effective replacement doesn't exist.

SnAu can be used in some cases, but clearly is too expensive for widespread use in, for example, MEMS capping.

This has not been for lack of trying, and several potential solutions have been explored. The Innolot project included such work.

Efforts continue and important new initiatives are underway in Europe and in Japan. The COST 531 consortium of more than 60 skilled European metallurgists has recently begun a new COST project to tackle the issue. The Japanese NEDO project is exploring a ZnSn option.

If this can be achieved then RoHS compliance will be simplified, since currently these products represent legal lead in an electronic assembly.

3. Lead-Free Finishes

Lead-free finishes existed before lead-free solders were introduced, mainly as advanced surface treatments for boards to give levelling or improve solderability. These were mainly NiAu, immersion Ag, immersion Sn or OSP. Some NiPd-based systems and Sn finishes were used in component finishes.

With the advent of lead-free soldering, lead-free finish technologies have been more widely applied to components and boards, displacing SnPb solderable finishes.

Whilst a number of finishes are in use for lead-free soldering, pure tin has emerged as a simple cost-effective solution for general use.

This has caused some alarm for those working with high-reliability products, particularly the US military and space sectors, where pure tin coatings had historically been prohibited on the basis of their propensity for developing tin whiskers leading to shorts. However, as detailed elsewhere, mitigation practices including thermal post-treatment of tin plated on copper provide sufficient protection against excessive whisker formation.

With several finish technologies alongside several lead-free solder technologies, the number of possible solder-finish combinations was large for compatibility studies. Very much of the early work in lead-free soldering technology was focussed on studying the effect of these combinations on solderability, joint strength, reliability etc.

In general, only Bi-containing systems emerged as having a potential compatibility issue with SnPb or Pb-contaminated lead-free solders. Thus, although it is more widely used in Japan, Bi is not yet adopted in Europe as a finish component.

Although there is a call for a single solution it is likely that a number of finishes are likely to continue to be used for various technical and/or cost reasons.

There have been examples of technology developments in the field. OSP finishes have been advanced to give sufficient robustness for multi-pass performance in the higher temperature lead-free processing environment. New low-cost immersion Sn processes were developed in the PRINT project.

Future breakthrough technologies would be required for to eliminate the need for use of expensive precious metals by matching low-cost solutions with the high performance needed in some applications.

Much attention has been focussed on the lead-free solder-finish interface in regard to both tin whisker formation and intermetallic growth and properties. These are critical to reliability, and new failure mechanisms are still being discovered.

New technologies could focus on a paradigm shift by which it is the substrate itself that is changed or modified rather than addition of an expensive finish layer to standard copper/steel substrates.

Study of intermetallic growth for nanoscale joints will become critical, as diffusion and reaction dynamics have a greater influence. Already there are electromigration issues in small flip-chip bumps.

4. Substrates

High Density Interconnection

Technology trends, both at the board level and the component packaging level are beginning to converge. With the advent of 3D systems, printable electronics and embedded devices, the concept of the basic 'Printed Circuit Board' is already changing.

Modern substrates are already multilayer constructions with complex interconnection pathways and advanced composite technologies.

As components miniaturise, interconnection configurations evolve and patterning/construction techniques change this trend could continue, until potentially circuitry is fully embedded and the concept of a substrate disappears altogether.

In the meantime, new technologies are required to meet the challenges of HDI (High Density Interconnection), including new ways to decrease conductor width spacing and decreasing plating hole diameter, for example.

As density increases, so do issues of interference and thermal energy management. The advent of interconnections for RF and optical signals will add complexity.

There are also important implications of the trend towards high density for inspection, testing and reliability, discussed below.

Electrochemical migration failure effects clearly have a greater potential influence for higher density interconnections.

The HDPUG (High Density Packaging User Group) has been focussing work for a number of years on these types of issues, including lead-free technology.

Thermal Degradation

The increased process temperatures for lead-free soldering have thermally challenged most polymeric materials used in electronics assembly, as process temperatures approach degradation temperatures.

For the most part basic research in lead-free soldering was carried out with small to medium-sized boards, where thermal degradation problems were only seen with temperature sensitive components.

More recently, as the IT/telecoms and aerospace/defence industries have been drawn into the transition, larger and more complex boards have been shown to have serious problems. The iNEMI group identified major issues with substrate warping and delamination and with repair and rework.

Substrate technologies have indeed advanced to meet the challenge and new 'lead-free compatible' products are now available. However, it is now clear that factors such as interlayer moisture, channelling and via density, for example, can play an important part and that it is not just a matter of good epoxy materials.

Recent work at IVF, Sweden and elsewhere has shown new evidence of wide performance variation in round-robin tests of substrates with delamination, warping and poor CAF results.

5. Halogen-Free Materials

The halogens bromine and chlorine are commonly incorporated into polymers used in electronics, either additively or as a part of the polymer structure itself. Such polymers are used in PCB substrates, component packaging, wiring, connectors, and casings as fire retardants.

Halogen-containing products have been under pressure for some time, with even PVC being targeted by environmentalists. The RoHS Directive specifically bans two types PBB's and PDBE's. However, whilst there is a general drive towards halogen-free polymers, the particular situation is made complex by the large number of different polymers and applications. Enforcement of legislation is also hampered by the difficulties in speciating to differentiate between legal and illegal substances.

The ~30,000 tpa. brominated fire retardants used in Europe is divided roughly equally between TBBPA, HBCD and Deca-DBE.

Deca-BDE is used mainly in housings, connectors, switches and capacitors. Although theoretically exempted under the RoHS Directive, a recent ruling by the EU Commission has effectively banned its use by implicating a Nona-BDE impurity. This issue is still mired in controversy but could have a very significant impact in development of new technologies in the short-term.

Halogen-free technologies for substrates include alumina trihydrate (ATH) and other inorganic fillers, red phosphorus and organophosphorus/organonitrogen compounds, but all of these have associated issues, including, for example, problems with mechanical and/or electrical failures.

Problems with stability in the z-axis and optimisation of µvias in terms of interface performance have also been observed.

Across the board the alternatives are more expensive than bromine. Also there is the doubt that phosphorus systems are indeed more environmentally acceptable than bromine.

There are a number of technologies that may be capable of cost-effectively replacing bromine, using nanocomposites with ZnSn or nanoclays, for example.

However, whilst it is still possible to use legal substances, industry will be reluctant to accept the costs of pursuing development and qualification of alternative technologies.

6. Underfills & Encapsulants

Underfill technologies are being adopted more widely. They are used to improve reliability for sensitive components under increased mechanical strains or for potting inside components.

Their use is also coupled with the increase in adoption of bare die technologies and this can be developed further.

However, their use is restricted by inability to carry out rework on the component should it become necessary. Technological progress may thus be focussed on underfill products that are reworkable, without land damage.

Other challenges include development of more user-friendly approaches, for example in a one-step application before reflow, or adoption of quick or no-cure systems.

The topic of conformal coatings is under review in Europe, led by NPL, UK. Preliminary work has shown that current coatings may be more permeable to dibasic acids from fluxes than previously thought, and that surface contamination plays an important role.

Industry feedback suggests that although there is a conservative attitude by some, others are anxious to fundamentally reassess conformal coatings technologies and develop new solutions.

The need for a wider industry consultation is indicated, with a common agreement on performance-led standards.

New technologies will need to consider a wide range of needs as well as basic barrier performance. These include eco-friendliness, the ability to deal with contaminant residues without requiring a cleaning step and the ability to rework/repair coatings on a localised basis.

7. CTE Matching

The new thermal issues generated by the introduction of lead-free solder processing has had and will continue to have a wide ranging impact on materials selection for electronics assemblies, particularly in high reliability products.

Further there is an increased focus on thermal issues in use, notably in harsh environments, for example automotive application. This is exacerbated by the greater localised heat generated in use by miniaturisation and greater integration.

The component mix is also becoming more complex, with a consequent introduction of more materials technologies and plurality of interconnection technologies. Optical PCB's are an example of the new challenges ahead.

The use of CTE (Coefficient of Thermal Expansion) matching brings a more thermally intelligent approach to assembly design, being in general the use of better thermal management techniques during processing and use.

These can be physical or structural technologies. An example of this would be the Alpha CoolCap, designed to shield temperature sensitive components during rework. In theory these types of techniques can minimise expansion of high CTE materials but in practice the board assembly is so complex that other parts of the board design may be adversely affected, for example.

Heat dissipation using conductive materials and channels may become more important.

Alternatively this could involve development and use of materials based on achieving CTE compatibility for adjacent materials to eliminate strain under temperature excursions.

A successful approach has been to design CTE-matched interposer layers of copper or other materials between die and substrate, for example.

The use of such interposers or 'transposers' can be effective, but again the knock-on effects on the whole board processing have to be accounted for.

FEM modelling can be used to assist in design, but in practice models are not particularly adequate and intuition is used with success just as often.

CTE acts in 3 dimensions although it is the xy of board plane, where the greatest challenges lie. Mismatch in the perpendicular z plane is crucial to reliability of vias.

Ceramics have a low CTE and high insulation and are used in high value high temperature applications. They are however expensive. Technological advances should include shrinkage control using predictive modelling and feature minimisation, with cost-effective higher quality products.

Via integrity during lead-free processing has been the subject of recent studies. It is possible, though challenging, to envisage the development of alternative via materials using polymers, other metals or ductile materials.

High Priority				
Issue	Challenges	R&D Needed	Notes	Target
	High reliability solders	Evaluation of the contribution of solder joint properties within holistic model of product reliability	Include mission profiles	2015
		Modification of SnAgCu alloys e.g. additions of ternary elements, nanoparticles to improve ductility, strength, improved sintering via nanoscience	Needs meaningful data and specifications	2015
Lead-Free Finishes	Low cost, high quality finishes	Development of Sn, OSP finishes to match flatness, barrier properties, durability of NiAu, Ag, Pd-containing solutions	Needs measurement values, quantified effects. Number of OSP reflow cycles e.g.	2010
		Development of combined immersion Ag/organic finish suitable for both soldering and wire bonding		2010
	Intermetallics control	IMC growth reduction technologies for drop test resistance, increased shelf life	Needs fundamental knowledge of IMC process	2015
Substrates	Thermally resistant laminates	Minimisation of warping during processing	Needs mechanism measurement methodologies	2015
Halogen-Free Materials	Non-Phosphorus fire retardant systems	New halogen-free fire retardant technologies for substrates, component packaging, cables e.g. ZnSn, Mo, nanoclays		2010
CTE Matching	Thermally compatible vias	New ductile polymer, metal materials for vias		2015

Medium Priority				
Issue	Challenges	R&D Needed	Notes	Target
Lead-Free Solders	Voiding control	Study of factors, types. location and effect on reliability		2015
	Cost-effective, reliable, low temperature soldering	Implementation of SnBi, SnZnBi and other Bi-containing solders		2015
	High temperature solders	Paradigm shift in component package design – no need for die attach, MEMS capping etc		2020
	Viable liquid solder interconnects	Development of alloys, component designs for high temperature applications		2020
	High speed, low energy interconnects	Integration of low resistivity materials e.g. metallic glasses		2015
		New technologies with anisotropic properties		2015
Lead-Free Finishes	Intermetallics control	New Cu-free substrate technologies – deposition process control		2010
		Effect of fast diffusion, miniaturised systems – IMC particle size, distribution control		2020
Substrates	Cost-effective high-density designs	New technologies for decreasing conductor width space, decreasing plating hole diameter		2015
	Thermally resistant laminates	New technologies for CAF mitigation		2015
		New technologies for delamination mitigation		2015
	Fully-embedded systems	Development of modifiable, repairable, reworkable embedded technologies		2015
		New technologies for metallisation, interconnection in meso-micro scale, 3D e.g. inkjet printing, selective micro-plating		2020
	Better understanding of properties	Characterisation of flex materials in relation to lead-free processing		2015
Underfills & Encapsulants	Reworkable underfills	New technologies for enabling rework, reuse of underfills		2015
	Better process integration	Development of one-part flux/underfill systems		2015

		New Quick/No cure underfill technologies		2015
	Improved conformal coatings	New robust, no-clean, eco-friendly, repairable coatings technologies		2010
CTE Matching	Better thermal management	New thermally efficient, low CTE, boards, packaging, underfill materials for process/use heat dissipation		2015
		New heat shielding technologies for temperature sensitive materials in processing		2015
	Wider use of ceramics technologies	New high thermal conductivity ceramics technologies		2015

Low Priority				
Issue	Challenges	R&D Needed	Notes	Target
Lead-Free Solders	Cost-effective, reliable, low temperature soldering	Modification of SnZn alloys to improve stability, processability, compatibility, reliability		2020
		Stable flux technology for SnZn solders		2020
		Substrate development for control of SnZn interfacial reactions, including oxidation mitigation		2020
	High temperature solders	Evaluation of ZnSn alloys		2020
		Non-IMC forming joining technologies		2015
Substrates	Better understanding of properties	Determination of mechanics of skin effects, surface roughness in FR4		2020
Underfills & Encapsulants	Improved conformal coatings	Mechanistic and performance studies of conformal coatings properties		2015
		Survey of current standards and industry agreement on a common performance-based test method for coatings		2015
CTE Matching	Wider use of ceramics technologies	Development of predictive modelling, feature minimisation to give better shrinkage control		2015

Process Technologies

1. Introduction

Process technologies for electronics interconnection are facing multiple challenges. Not only are assembly materials changing, but designs are increasing in interconnect density, components are becoming smaller and component mix is increasing. All this with pressure to reduce costs.

In general the trend is towards greater process control. For example lead-free soldering requires a narrower process window, ultra-small components need more accurate placement and selective soldering could benefit from greater automation.

There has also been a demand for new guidelines, for example in lead-free soldering, particularly from SME's who need urgently to benefit from the experience of others.

A key current technology need in lead-free soldering processing is for a greater understanding of manual soldering, especially in relation to rework and repair. Most of the previous work in lead-free soldering has been with wave or reflow soldering, with little published information on hand soldering thermal management, quality control and effect on reliability.

New thermal issues associated with large and complex boards require urgent solutions. This will become more acute as affected industries such as aerospace and IT servers adopt lead-free technologies over the next decade.

Compatibility issues are still being addressed in lead-free technology, specifically in mixed assembly with both SnPb and lead-free solders present, notably BGA-related wetting.

Miniaturisation will test the microscale boundaries of soldering technology and some important work is ahead.

Bare die technology still requires process developments.

New technologies including jetting, dispensing, laser and vapour phase soldering are in development although their impact remains to be seen.

2. Lead-Free Soldering

Wave & Reflow Soldering

Wave and reflow soldering are the major mass soldering techniques used for electronics assembly and have been the basis for most lead-free soldering research.

The basic lead-free soldering collaborative experiment was first carried out in large scale in the mid-1990s as the IDEALS project. The IMECAT project is an example of a more recent action looking at automotive, telecoms, displays and smart card applications in more detail.

SME-focussed activities began in Scandinavia with the NoNE project as a major part. Later EU the projects LEADOUT, GREENROSE and LFS-for-SME's widened the scope of such work.

From an industry perspective much of the early work was initiated and supported by solder manufacturers in customer trials. CEM's and OEM's across the world have now implemented the technologies on a fully commercialised scale.

The major issues were associated with the higher processing temperatures and narrower process windows. Evaluations were of different solder alloys in combination with the various lead-free finishes, looking at printing, wetting, joint strength and reliability, for example.

Much work was done on the reflow heating profile and also on the issue of wave solder bath erosion. Equipment manufacturers now have advanced knowledge and solutions. There is still some development in design of heating and cooling zones for reflow as well as some interesting work on advanced stencil technologies for reflow, for example.

Given the relative maturity and knowledge of the basic technology it was surprising in 2005 to see some results from iNEMI, US with larger and more complex boards, that showed significant damage from component and board stress in multiple pass experiments. This also relates to other recent work mentioned showing issues with laminate stability, via cracking and hole filling. This may be due to the fact that most of the basic work has been done with small or medium-sized boards, rather than the larger boards used by sectors such as aerospace and defence currently exempted from the RoHS Directive.

These sectors are also affected by the issue of mixed technologies, where SnPb and Pb-free materials are mixed, perhaps inadvertently, on the same board. Here work at NPL and elsewhere has shown that in fact some levels of Pb contamination in the lead-free process can even be beneficial. In general though mixed assembly should be avoided. However, success is product-specific and SnPb components can be used in lead-free assembly. This can also work vice versa, provided that careful attention is paid to components such as Pb-free BGA's, requiring sufficient solder paste volume and temperature to ensure complete dissolution.

Use of nitrogen to reduce drossing and improve wetting was much debated in the early days. It is now accepted that it

is not essential but beneficial, particularly for the larger and more complex boards.

Some work has been done on the effect of cooling rate on joint stability, e.g. in the EFSOT project, but perhaps this area has not been fully explored to give insight into effects on reliability. In particular attention should be paid to real-life conditions and simulations must match these as closely as possible, since there are many relevant factors. Given the complex nature of the lead-free alloy microstructure and the strong effect of interfacial reactions, especially for small joints, an adequate study could be extensive.

Future challenges in wave and reflow soldering may be related to faster and more flexible equipment setup, more energy-efficient operation, integration with a wider component mix and with ancillary operations, and miniaturisation.

Hand Soldering

Hand soldering with lead-free solders was a rather neglected yet important area of research, probably due to the focus on mass soldering techniques. It has a particular relevance to selective soldering and repair/rework and is in fact widely used, particularly amongst SME's.

An early identified issue was greater tip wear of soldering irons using lead-free solders. This is now well-understood.

The first and only major collaborative project to address manual soldering specifically was LFS-for-SME's, recently concluded. This highlighted the need to retrain operators for the significantly different heating protocols and wetting behaviour with lead-free solders. These have been key parts of training courses offered by consultants.

Surprisingly the reliability of manually soldered lead-free joints has not been comprehensively studied, with largely empirical and often contradictory reports. Such a study should benchmark a wide variety of materials and assembly operations with different operators. Repetitive operations are particularly of interest.

Repair & rework is the area that has recently attracted much attention, again for larger boards. Here it has been shown that there can be significant issues with copper dissolution and damage to adjacent components arising from the difficulty in localising the large quantities of input heat required. A major OEM recently evaluated a number of repair and rework stations and found a majority were inadequately adapted for lead-free soldering. Reproducibility of hand soldering is always a source of failures.

More work needs to be done to develop advanced technologies for better heat control and localisation. This would be assisted by more thermally intelligent design of assemblies to allow for the needs of repair/rework operations. New flux technologies for better hole filling are already becoming available. Greater use of robotics may be seen.

A non-technological but nevertheless important issue for repair/rework is that of product labelling, With the large variety of materials and materials combinations is use and the sometimes extended timescales involved, it will be increasingly necessary for operators to be able to identify materials accurately and so avoid potentially serious compatibility issues.

3. Heterogeneous Assembly

At the convergence of lead-free and miniaturisation technologies there lies a very significant challenge.

Smaller and finer pitch joints require advanced solder paste technologies with good wetting properties. However, the new lead-free solder pastes are still in transitional development and their wetting is generally poorer than conventional SnPb.

Extensive work on ultrafine pitch lead-free solders was carried out in the UK with flip-chips. A process route for sub-100 micron pitch was identified. The project required advanced stencil design and manufacturing development as well as use of an at the time leading-edge ultrafine Type 7 solder pastes.

More recently the new challenge has become heterogeneous assembly – the assembly of both very large and very small components on the same board. This fits well with a new drive in MNT (Micro-Nano Technology) manufacturing and use technologies generally towards heterogeneous systems.

A large consortium has been assembled in Europe, led by ELFNET, to carry out a collaborative project.

The challenge is extreme and will require a radical revision of the basic printing and soldering experiments. The work is expected to advance lead-free soldering science in general.

New solder pastes and associated materials will be required, probably using up to Type 8 pastes, but with rheology capable of simultaneously joining large and small components.

Stencil printing and associated technologies such as dispensing and cleaning will need to be advanced. At the same time better measuring techniques for printed solder paste volumes will be required.

The processing steps itself is possibly the most difficult, with ability to achieve much better control of localised heating to match the heterogeneous thermal requirements of very large and very small components. Perhaps integrated heating elements in components or on the board could be envisaged, or even in the longer term micro-robotic units.

Long-term reliability and ageing of such solder joints will also have to be evaluated.

4. New Process Technologies

As the soldering process becomes more complex and manufacturing/automation processes advance it is inevitable that new process technologies will be explored and implemented in niche applications at least.

Vapour phase soldering is an adaptation of reflow soldering using volatile liquids to stabilise and homogenise the process temperature within a narrow window. It is generally a small-scale batch process. It is not a new technology and indeed was largely dropped, mainly due to negative environmental perceptions of the liquids used. However, with the advent of lead-free soldering and its particular need for better thermal control in the processing, it has re-emerged somewhat. It may be particularly suited to heterogeneous assembly of very small and very large components, since in principle it equilibrates surface temperatures.

The LFS-for-SME's project has significantly advanced the vapour phase technology. A continuous inline process has been engineered and vapour emissions minimised. There is a great deal of interest in this development and the suggestion that further developments are likely.

Laser soldering offers interesting new possibilities for a non-contact localised heating control. Its implementation requires development work in greater understanding of the resulting joint structures and microstructures, and their reliability. There are also safety concerns that may need to be addressed for operators.

Again the LFS-for-SME's project has developed the laser soldering technique. A handheld unit has been designed using a CCD camera to safely guide operator use and a thermal feedback system used for temperature control at the joint surface.

JOITEC was a parallel project also looking at a new laser soldering technology.

Jetting & dispensing techniques are likely to undergo rapid development in the next few years, coupled with the drive for printable electronics and more controlled deposition methods generally. Robotic dispensing is likely to become a standard technology in the near future, whereas jetting may remain a niche process.

Novel process concepts include the use of a micro-welding technology to produce a metal droplet from a wire. DROPLET WELD, completed in 2002, examined the use of a laser to produce higher droplet rates and smaller drops. A single laser was used to drive multiple welding stations for low cost welding.

5. Process Optimisation

General guidelines for lead-free soldering process optimisation have been and will be made available through the several SME-based projects mentioned above. Knowledge is also disseminated on various websites and via solder and equipments suppliers.

However there is a need for much more detailed and specific application-based guidelines. There are a wide variety of options and possible materials combinations, for example, and it is desirable that these be narrowed and tailored for relevant assembly types.

Given the uncertainties about reliability it will be some time before these can be confidently substantiated with reliability data but this remains an objective.

As in any manufacturing process optimisation decreasing the number of process steps is desirable for greater cost and time efficiency.

This need also arises in modern electronics assembly from the increase in component mix and more non-standard end-of-line steps such as underfill or depanelling. Increased addition of optoelectronics, oddform and connectors brings the need for more selective soldering and the opportunity for exploitation of automation and robotics.

Old and new concepts for achieving this include no-clean technologies, integration of the underfill step with standard processing and snap-in assemblies, for example.

Other developments may include data feedback with design systems and innovations in placement technologies for rapid reconfiguration and use with higher density assemblies.

Bare die technology offers some significant advantages in process optimisation but still has barriers to full implementation. Handling, especially in placement needs to be improved for example. The ‘Known Good Die’ principle has been used to mitigate quality issues, but there must still be questions about attachment reliability, testing, repair and rework. New materials for underfill and encapsulation are desirable.

High Priority				
Issue	Challenges	R&D Needed	Notes	Target
Lead-Free Soldering	Effective rework and repair	New heat management technologies to mitigate colateral damage	Deployment of state-of-the-art	2010
		New techniques for reduction of metal dissolution – Cu, Fe	Ibidem	2010
	Processing large and complex boards	Improved technologies for hole filling	Evolutionary development will solve in 3 years. Cost an issue.	2010
	Low temperature soldering	New energy efficient, low temperature soldering methodologies and equipment	Total energy consumption must be measured	2010
Heterogeneous Assembly	Improved printing technologies	Advanced printing technology(s) for one-step printing of differing paste compositions e.g. jetting, multihead jetting, robotics		2015
	Heterogeneous processing	New technologies for localised heat variation and control during mass soldering processing	Special solutions exist – deployment to state-of-the-art	2010
New Process Technologies	Faster, more cost-effective laser soldering	Expansion of scope to include larger BGA's	How do lasers reach underneath?	2010
		New solder paste technologies to match laser heating profiles		2015
		Integration of laser soldering into existing assembly equipment/ processes	Integration must be economic	2010
	New concepts for direct interconnect	Development of solid state joining technologies – bonding (thermocompression, ultrasonic, thermosonic), builtup joints (PVD, CVD), electroplating etc.		2015
Process Optimisation	Decreased process steps	New automation technologies for cost-effective selective soldering	Possibly economic for low volume production	2010
	More process control	Development of assembly data collection and realtime feedback to design, QC testing		2010
		Improvement of placement accuracy for high density assembly	Current accuracy (45 µm 4 Sigma) – adequate for existing technologies	2015

Medium Priority				
Issue	Challenges	R&D Needed	Notes	Target
Lead-Free Soldering	Effective rework and repair	Improved on-board labelling, tracking of materials	Deployment of state-of-the-art	2010
		New technologies for rapid localised heating		2015
	Processing large and complex boards	New thermally intelligent board, component designs including localised heat shielding, dissipation, minimised hotspots		2015
	Reliable mixed SnPb/Pb-free assembly	Guidelines for SnPb/Pb-free mixed assembly		2010
Heterogeneous Assembly	Customised solder pastes	Development of advanced type 3 - type 8 solder paste formulations capable of use in simultaneously joining very large and very small components		2015
New Process Technologies	Faster, more cost-effective laser soldering	Development of faster, non-sequential methodologies	Integration must be economic	2015
	Wider adoption of Vapour Phase soldering	Development of faster throughput, large scale systems		2015
	Cost-effective jetting & dispensing	Advanced robotic technologies for fast high quality delivery of solder pastes / melts		2015
		New technologies for inkjet printing of solder patterns		2015
Process Optimisation	Improved Bare Die technology	Studies of test, repair/rework and reliability issues		2010

Low Priority				
Issue	Challenges	R&D Needed	Notes	Target
Lead-Free Soldering	Effective rework and repair	Better process and quality controls	Deployment of state-of-the-art	2010
		Retraining for operatives in lead-free technology	Ibidem	2010
		Development of product/assembly specific rework tools and methods	Ibidem	2010
	Reliable manual soldering	Reliability studies for repetitive manually soldered joints		2010
		Workmanship standards for manual soldering		2010
Heterogeneous Assembly	Improved printing technologies	Fundamental study of solder paste behaviour in stencil printing		2010

		New automated measurement technologies for deposit size/volume		2010
		Development of enhanced stencil printing technologies – stencil treatment, multilevel stencils, vibrating squeegees, ultrasonic dispensing, automated cleaning		2010
New Process Technologies	Wider adoption of vapour phase soldering	Studies of reliability of joints compared to conventional systems		2010
	New concepts for biodegradable joining	Feasibility studies with new technologies for forming biodegradable joints, characterise mechanism		2020
Process Optimisation	Better Guidelines	Dissemination of process guidelines for each alloy, application, plating combination, supported by reliability data		2010
	Decreased process steps	Development of pre-reflow, integrated underfill systems		2010
		Development of efficient, low-stress depanelisation technologies		2010
		New technologies for elimination of cleaning processes		2010
	More process control	New technologies for data transfer from design systems to placement systems		2010
		Optimisation of placement methodologies for rapid reconfiguration		2010
	Improved Bare Die technology	Development of improved handling methodologies		2010
		New methodologies for integration with existing process systems – placement, followup operations		2010

Testing & Reliability

1. Introduction

The highest profile and priority of all lead-free soldering technology issues currently is that of reliability. Much of the initial work has focussed on consumer or communications applications but attention is now turning to sectors still working to implement the technology such as automotive, aerospace, IT servers and medical devices. In all of these there is a safety-critical need for high reliability of electronics interconnection.

In fact there is a considerable body of data to show that lead-free solder joints can be stronger than SnPb and indeed this was the reason for its early use in automotive under-bonnet applications. However, the abundance of data generated since has shown a complexity and contradiction that has given concern.

In general it appears that current reliability test methods are not robust enough to comprehensively accommodate the paradigm shift involved in introduction of the new lead-free technology. There is an urgent need to resolve the multiplicity of new factors and failure modes and develop new tests. There are no adequate models for long-term reliability.

Important work is now under way to exchange reliability test data and to harmonise test methods. This also considers quality issues.

More electronics are being used in harsh environments and this is challenging interconnection technology.

Further, the boundaries of what is possible are being approached in terms of quality and functional testing for miniaturised systems with fine pitch arrays, high density interconnection and embedded systems.

Testing of the anticipated nanoscale or biological devices is little more than conceptual at present.

More work is also needed to integrate testing with assembly, inspection and supply chain data exchange.

2. Inspection & Test

The move towards high density interconnection and packaging brings an obvious challenge to test methodologies.

Test access is one specific example, in which it may not be possible to gain access to connection points for, for example, arrays with <200 um pitch for functional testing.

Embedded systems bring their own challenges including long-term drift.

In general, these challenges mean that testing protocols will need to be adapted to change. For example, restrictions on diagnostic intervention mean that good processing becomes more important, with a strong reliance on a successful end test. Unassembled electrical testing becomes much more important for high density products.

Clearly advanced cost-effective non-contact technologies are required; probably developments of the boundary scan technique.

Integration of new photonic and RF interconnections is likely to require adapted or new testing technologies. Nanoscale, biological and plastic electronics will also challenge testing techniques.

As assemblies move towards 3D form factors and interconnection, with increased layers and stacking, visual inspection restrictions will increase. New technologies, for example high-resolution automated X-Ray inspection, will be required.

3. Reliability Testing

As lead-free soldering technology matures, the lack of knowledge in reliability testing has become probably the most acute issue, especially for high reliability sectors such as aerospace, currently exempted from the RoHS Directive.

This issue is a complex one, since the fundamental science relies on a detailed knowledge of joint and materials properties at the microscopic level, advanced computing, process information and good understanding of the mission profile.

Modelling and simulation approaches to the issue are described above.

The real issue here relates to the raft of empirical test methodologies designed to simulate the real-world product mission profile using standardised test pieces. This includes drop testing for mobile devices, for example, where the test board is dropped from a specified height a number of times. Thermal cycling, with or without vibration and humidity control, is a commonly used standard for electronics assemblies. Electromigration tests are also important.

More recently there have been moves towards combining tests to reduce cost and increase data output.

These tests have been designed and developed over a number of years and continue to evolve to greater sophistication. However, technology has been based on SnPb solder joints and the significantly different mechanical properties of lead-free solders have necessitated some radical revisions.

Lead-free solders are, of course, of several different types, each with differing and complex microstructure, interacting in different ways with substrates and sometimes with different failure mechanisms.

In studying these factors and attempting to adapt testing technologies to lead-free soldering, there has been a plethora of work on new customised apparatus and test protocols. Whilst these are useful in producing comparative data within the specific modality and environment of the test, important questions about relation of the results to real-world performance remain. Further, such customised tests will always be non-standard, whilst there is no agreement on new reliability standards.

The only realistic resolution is for experts to meet and agree a harmonisation of test methods. This is underway in Europe in ELFNET. Several meetings have taken place and a ‘Colour Book’ is being produced.

A French group, EURELNET, also has the same objective. Also, US Aerospace industry leaders have met, under the guidance of AIA and GEIA, to collectively consider reliability test methods. It is clearly desirable that all such efforts are coordinated globally.

The ELFNET group has discussed the topic from a radical perspective, considering the very basis of the reliability concept, as well as attempting to distinguish between reliability and quality testing. There is an increasing awareness that a view considering only the joint itself is not sufficient, since material and geometric factors of the assembly itself also play a key role. This leads to a more

empirical approach, with greater focus on the mission profile.

ELFNET has listed and categorised all known failure mechanisms, considering each separately in the question of appropriate test methodologies.

The multi-factor reliability behaviour of lead-free soldered assemblies gives rise to very significant variation in test results. Thus although broad patterns are distinguishable, it is quite possible to show example of contradicting data. ELFNET and others have created collective databases using various contributors to highlight trends, with variable success. This requires significant resource and goodwill inputs from cooperative parties and has also issues related to confidentiality.

Many are calling for collation of real-life field data on failures types, lifetimes etc to feedback into research programmes. Again, however, this is hindered by the nature of such a task, as well as the immaturity of technology use. Ways to achieve this are urgently required.

Long-term reliability - normally defined as greater than 5 years lifetime – is a particularly fraught topic. All testing must be accelerated and predictive at this level and thus all of the uncertainties above are exaggerated. It has been said that “we are at zero” in this field for lead-free, with missing models, standards and experience.

In fact, long-term reliability for SnPb joints had not been solved before introduction of lead-free technologies.

New statistical processes are needed to generate acceleration factors.

The effect of ageing cannot be accurately assessed. Although there are many test methods there are no comparative models. Physics of failure needs to be applied.

4. Tin Whiskers

Tin Whiskers Standards

The phenomenon of tin whiskers was well-known before the introduction of lead-free solders. Tin coatings on components were banned from US military applications for this reason, resulting from suspected cases of failures of satellites and other devices due to spontaneous whisker formation.

As lead-free soldering was implemented it became apparent that pure tin coatings were the simplest and most cost-effective general lead-free alternative. This has driven an intensive effort to better understand the mechanism of formation and means to mitigate the behaviour.

Given that the science was extremely complex, an empirical approach to a test method standard was required to facilitate a speedy lead-free transition. Four major research teams worked together towards a global approach – JEITA, Japan, iNEMI, US, Soldertec, UK and the E4 PROTIN project in Europe. Several alternative methodologies were evaluated, with reference to known factors such as substrate type and stress modes.

JEDEC issued a revised standard JESD22A121.01 in October 2005, using three test conditions – two isothermal conditions with controlled humidity and a thermal cycling method.

The IEC is currently in the final stages of approving IEC 60068-2-82 Ed 1.0, for release in early 2007. This also has three tests – ambient, damp-heat and thermal cycling.

Although these standards provide guidance to acceptance criteria, they do not standardise them. In principle they provide methods to accelerate and characterise whiskers, but are inadequate to quantitatively predict whisker growth over a long time period and have no necessary correlation with real-life service behaviour.

An approach towards acceptance criteria has been subsequently produced by JEDEC in cooperation with E4, iNEMI and IPC. This has been included in JESD201, released in March 2006. Test duration and acceptance criteria are defined in product classes and for change acceptance.

High reliability groups in iNEMI and GEIA have produced guidelines and standards based on mitigation of tin whisker risk, rather then a formal assessment of whisker formation.

It is likely that these standards will continue to be revised in the light of further experience. In general, although it appears that standardisation is reaching maturity, there is still a need for global adoption of a unified set of test methods and acceptance criteria.

Concern from the high reliability sectors may be lessened in the short term by approval of a recent RoHS exemption for lead in tin coatings for fine pitch components (<0.65mm), though there are questions now about its relevance.

Mechanism of Whisker Formation

The work on standards has very significantly advanced understanding of tin whisker formation and has been accompanied by much proprietary work by plating specialists to make whisker formation a far less likely occurrence than some years ago.

However, the exact mechanism is still controversial and fundamental research work is likely to continue for many years.

Work to find ways to accelerate whisker growth for testing and qualification is important since current tests are onerous, with long durations.

It is known that important acceleration factors include the substrate used, the plating chemistry/process used and stresses within the coating.

Mitigation thus includes avoidance of 'bad' substrates, use of a barrier layer such as Ni, a small amount of alloying, reflow or annealing to remove stresses and careful selection and control of plating.

More recently it has been shown that conformal coatings may be able to suppress whisker formation. There is also some evidence that roughening or etching the copper surface can have a positive effect. Another example of recent work studies use of Cu6Sn5 precipitates deposited at the grain boundary to block diffusion of tin.

IBM has published a history of tin whisker theory to 2004 and iNEMI has several available papers illustrating the differing theories.

Groups such as iNEMI and CALCE in the US continue to work in this area. NASA hosts a leading website on the issue. ELFNET maintains an expert group on the topic with a web/email forum.

Areas for future research include aspects such as whisker strength and resistance to mechanical shock and vibration.

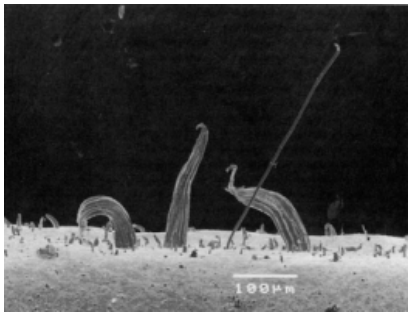
In general the field is likely to evolve in the direction of advanced plating technologies. This includes the use of binary or ternary alloys and composite coatings using codeposited organic and/or metal particles.

Microstructure tailoring of the tin layer may be possible, using current modulation, such as pulse plating. The objective is change the grain structure from the standard columnar morphology to a so-called equi-axed structure, which is thought to be a safeguard against the grain boundary sliding mechanism thought to be involved in whisker formation.

Long-term performance results and field studies for currently acceptance criteria are needed.

Collaborative funded research in Europe is somewhat hindered by the very significant proportion of work carried out as proprietary research, or within large relatively closed industry groups such as E4 and iNEMI.

Nevertheless, a fundamental understanding of whisker growth is essential to the development of reliable mitigation practices and prevention strategies, enabling larger use of tin-based finishes.



5. Harsh Environments

All of the issues related to new materials and reliability detailed above are rendered more acutely within harsh environments. These are typically found in the transport industries – automotive, aerospace, railways, for example – as well as the oil industry, submarine environments etc.

ELFNET maintains an expert group on the topic, with several partners engaged in relevant projects. The HITEN3 European network specialises in high temperature electronics. In the US CAVE at Auburn University specialises on automotive electronics.

The challenges posed to reliability of electronics assembly in these extreme environments are severe generally and now complicated by the introduction of lead-free soldering and other new technologies. Equipment is required to be durable under high temperatures and pressures, with vibration, shock, contamination and/or corrosion.

All of the issues mentioned elsewhere are relevant to technology advances in harsh environments. CTE and packaging optimisation will need attention. CAF defects in substrates, for example are likely to be more common. High temperature resistant, ductile solders are required with reduced content of brittle intermetallics.

Reliability modelling and testing will have to be more specifically focussed on the mission profiles, perhaps with a product-specific approach to account for the wide variety of harsh environments. At the same time environments should be defined, categorised and simplified.

New design and technological approaches for harsh environments could be envisaged.

Conformal coatings are a topic of particular relevance, but this could perhaps be extended to consider other ways of completely encapsulating assemblies for protection from the environment.

More consideration could be given to strategies for minimising damage to assemblies and its effects by, for example, moving towards low energy/voltage systems, or introducing new interconnection-based approaches to redundancy.

In the longer term, with the development of molecular and nanoscale electronics, new technological approaches could be envisaged using, for example, remote robotics or self-repair materials, that would be used for isolated and remote environments such as submarine oil drilling.

High Priority				
Issue	Challenges	R&D Needed	Notes	Target
Reliability Testing	Harmonised test methods for lead-free technology	International, European expert networks with communication and data exchange tools for cooperative action	Specify, define of data aspects. iNEMI, CALCE, ELFNET coordination	2010
		Reconsideration of reliability and quality definitions for electronics interconnection – development of mission-based, physics-of-failure approach. Lifetime prediction model. Product emulator(s)	EU coordination necessary critical	2010
		Collaborative exercise to collate field failure data	Need to define methodology	2015
		New methodologies for assessing reliability including new tailored accelerated test methods, models and protocols, pass/fail criteria based on real-life experience	Determination of physics-of-failure. JEITA will propose new IC standards.	2010
	Lifetime prediction	Application of statistics to unified data sets to create models, define acceleration factors, ageing	Standardised methodology needed for specific tests. Database needed to verify prediction tools but data is proprietary.	2010
		New standards for predictive failure	JTAG, IPC, JEITA, IEC? Industry validation group	2010
Tin Whiskers	Global harmonisation of tin whisker standards, guidelines	Globally cooperative exercises to further refine, customise tin whisker standards for test strategies, acceptance criteria, mitigation practices		2010
		Design techniques, rules for whisker mitigation		2010
	More focus on component finishes	New whisker-resistant substrate technologies		2010
	Improved understanding of tin whisker behaviours	New studies of interfacial phenomena, intervention methodologies.		2010
		New studies of tin whisker strength, effect of mechanical shock, vibration		2010
		Collation, evaluation of real-life field data to assess mitigation practices.		2010
		New studies of effects after processing - bending, joining		2010

Medium Priority				
Issue	Challenges	R&D Needed	Notes	Target
Inspection & Test	Effective High Density testing	New technologies for inspection and testing of embedded components e.g. automated X-ray		2015
		New methodologies for unassembled electrical testing		2015
		New micro-nano scale test access techniques		2020
		Design for boundary scan testing	JTAG	2015
	Adaptation to new technologies	New approaches for evaluation and testing of biological, molecular electronics		2020
Tin Whiskers	More focus on component finishes	Use of mission-critical selection procedures		2015
Harsh Environments	Robust, durable electronics	Development of low voltage systems		2015

Low Priority				
Issue	Challenges	R&D Needed	Notes	Target
Harsh Environments	Robust, durable electronics	New technologies for complete encapsulation of assemblies		2015
		New approaches to redundancy on the macro-scale		2020
		New technologies for remote, self-repair – materials, nanorobotics		2020

Sustainable Electronics

1. Introduction

The advent of the RoHS Directive is by no means the beginning or the end of the topic of ‘green electronics’. Very significant work has been underway for more than a decade on eco-design and recycling technologies for electronics. The WEEE Directive has not yet fully impacted recycling, disassembly and reuse technologies on an industry scale. Ahead are the REACH Directive and the EuP Directive.

All of this is likely to escalate the debates currently in progress on government regulation vs. legislation, global government policy consensus and the business case for introduction of environmental technologies.

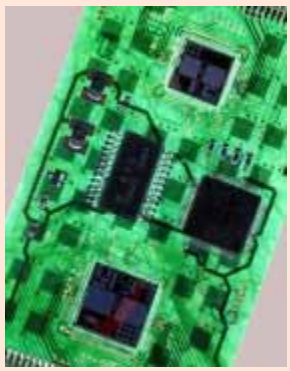
Already questions are being raised about the existing Life Cycle Analysis (LCA) data theoretically supporting the transition to lead-free soldering, for example, and this needs to be addressed further.

However, the pressure is likely to increase and it is thus vital that new technologies provide an economic benefit to conforming. There must be a business efficiency reason for recycling electronics, for example. Design for disassembly and disassembly technologies themselves must contribute positively to the cost equation.

Plating processes for board and component finishes are generally considered to generate the most significant EHS issues due to the large amount of water, chemicals, energy and waste involved. Important progress has been made towards closed-loop systems and recovery of metals for reuse.

In the assembly process itself focal points already include the fluxing and cleaning processes. It is likely that energy use will also be considered in greater detail and lead to new equipment designs.

There is growing pressure to develop reuse technologies for components, but significant industry reluctance to consider this option.



2. Life Cycle Analysis

Life Cycle Analysis (LCA) will grow in importance to justify use or non-use of substances in electronics as well as in industry generally. Sustainability pressures are growing in Europe, enhanced by the recent introduction of the REACH Directive, for example. Risk assessments, data collation and impact assessments will all become common currency, involving the complete supply chain.

A recent industry article speculates that competitive strength at conducting life cycle analysis will be a "key survival factor".

These studies are on the one hand used by environmentalists to support banning or restriction of target substances. At the same time industry may want to use the same work to justify continued use. Thus LCA work can easily become politicised and controversial.

This has already happened in the field of lead-free soldering technology. Major LCA studies have been carried out, including the European EFSOT project and work by the EPA, US in which some European parties were involved.

However, there has been a significant lack of confidence in some of the data, since much has to be estimated rather than measured. Further, there is still a perception of lack of clarity on relative weighting of the various factors such as emissions, toxicity, energy etc.

New models and metrics are required to more confidently typify the electronics industry. For example, 'life cycle' in the aerospace industry is taken to be 30 years, whereas in the consumer industry it is 30 months.

Work on data collation needs to continue, with as yet key data still missing. An obvious example is the total amount of solder used in electronics – until recently only guessed at. Data on tin mining and tin emissions is only now being collected by the tin industry.

Recommendations for improvement of LCA studies formed part of the ECOLIFE II Summary Report of 2003.

Future work in this area needs to involve a more collaborative approach, inclusive of all major stakeholders and in liaison with policymakers. European experts need to agree on the basis for the work, the methodologies and the interpretation on which work is to be carried out, within an open and publicly accessible framework.

Only with such an approach can results gain credibility, ownership and scientific accuracy.

3. Recycling & Reuse Technologies

Research in WEEE recycling has been in progress for more than a decade. ELFNET has reported more than 100 projects in Germany alone. Numerous innovative processes for recovery of metals and other materials from electronic assemblies have been developed and WEEE recycling is now a commercial fact.

However, there is still a perception that the business case has not been truly made for recovery or reuse of electronics waste. Whilst the WEEE Directive is focussing minds, there has ultimately to be a cost benefit for industry.

There is some scepticism that the energy/pollution/cost balance can in fact become negative for large-scale recycling.

Certainly existing processes recycle on a commercial scale, using electrolytic or other technologies. Usually the economics is based on recovery of precious metals – Ag, Au and Pd - from surface finishes and now Ag from lead-free solders. Expensive components can be recovered using sometimes sophisticated processing such as infrared desoldering with robotics.

Data for specific technologies such as flip-chips or plated plastics would be desirable.

Greater use of thermoplastics would enhance recovery of useful materials, though there are questions over performance and costs.

A top priority issue is labelling of electronics assemblies and products with hazardous substance information. This is a requirement for the WEEE Directive, enabling recyclers to cost-effectively process WEEE. It is also an explicit requirement of Japanese and Chinese regulations. Standardisation is required as are technological advances in data transfer, based, for example on RFID.

Discussion of the reuse of WEEE is principally focussed on components themselves, though in theory this could be broadened to include the electronic assembly or indeed the whole product, should it survive the disposal process. Reuse of PC's is probably the most common example of the latter.

In regard to components, there are current commercially operated technologies for desoldering and retinning components, usually focussed on premium actives.

There are significant issues around training of operators, role of intermetallics, reliability degradation and warranties.

Electrical testing and qualification of such components must be done against specifications that may be only available from the original supplier, if the part is not obsolete.

Generally such components are not reused in high reliability applications in Europe.

To resolve these issues requires new specifications and standards, allowing more confidence with regard to warranties and performance.

New Design for Disassembly technologies are required for rapid and cost-effective disassembly and reuse. It is likely that this will increase the modularity of designs and also the use of technologies such as snap-in assemblies.

4. Eco-Design

Eco-design for electronics is not a new topic, but one that is set to dominate future design philosophies.

The earliest collaborative initiative was probably GreenPack in Scandinavia. The Eureka CARE electronics initiative has just finished. There are several leading European centres, including CfSD and Fraunhofer IZM, In 2005 the Commission sponsored an Eco-Design roadshow aimed at raising awareness of SME's to the issues.

Eco-Design will seek to redesign both products and processes to minimise environmental impact across the board.

Electroplating processes, supporting both substrate and component manufacture, has arguably the most significant issues in regard to impact, utilising, emitting and disposing of large quantities of chemicals, as well as energy. For some years now technological developments have focussed on developing closed-loop systems and this should continue.

Tin stripping is a focal point, in which tin is electroplated and then stripped off substrates within the same process. Studies are currently looking at ways to recycle and reuse water and acids, for example. Reclamation and reuse of the tin sludges is challenged technically and is perceived to lack an economic incentive.

Inevitably too the energy use in soldering processes will need to be addressed. New technologies for low energy and reusable energy soldering are required. The NoNE project showed that initial oven heat to higher temperatures takes 70% more energy, but the power increase to maintain higher temperatures is only 15%. This was some years ago and today's equipment may have lower margins.

EcoDesign will radically simplify and reduce the variety and particularly the amount of materials used in electronics, with consequent impact on the supply chain, converging with consumer pressure for smaller, lighter and more functional products.

In a recent industry article it is claimed that owing to the reductions in hardware mass, the number of producers, raw material options, and component and circuit board suppliers will reduce as well to as low as 10% of today's number.

Materials that are used will increasingly be fully characterised through LCA and many replaced by eco-efficient alternatives, for example compostable materials.

The list of target substances is likely to expand well beyond the six RoHS elements, and industry will need to work even harder to ensure and highlight the scientific bases for such moves. In the automotive and plastics industries Sb use has been under pressure for some time. The increased use of Bi and Ag in lead-free solders has already attracted attention.

High Priority				
Issue	Challenges	R&D Needed	Notes	Target
Life Cycle Analysis	Accurate, meaningful LCA results	New LCA models for electronics interconnection	30 years for high reliability – cf. 30 months for consumer!	2010
Recycling and Reuse Technologies	Low cost electronics recycling	Development of new design concepts, standards, techniques, materials for rapid disassembly	Need disassembly, reuse definitions, targets e.g. 1% new consumer by 2015	2010
		New methodologies, designs with reduced part counts, material mix		2010
	Reliable reusable components	Study of the effects of desolder-solder, retinning on reliability	Services available. Cost an issue.	2010
		New technologies for component retinning, array reballing using PbSn - for high reliability applications	Services available. Cost an issue.	2010
Eco-Design	Eco-efficient electronics assemblies	Studies of environmental, toxicological impact of non-RoHS elements in electronics – Ag, Bi etc	Some studies exist. Will be a part of REACH	2010
		Studies of EuP compliance impact, emphasis change		2010

Medium Priority				
Issue	Challenges	R&D Needed	Notes	Target
Life Cycle Analysis	Accurate, meaningful LCA results	Studies for generation, collation of missing datasets – mass flow volumes, toxicology data, mining data, disposal issues	UK network SUMEEP	2010
Recycling and Reuse Technologies	Low cost electronics recycling	Development of technologies for greater use, recovery of thermoplastics		2020
	Reliable reusable components	Development of industry guidelines, standards for reuse, labelling, warranties		2015
		New design concepts, techniques for electronics assemblies with reusable modules, snap-in assembly		2020
Eco-Design	Clean electroplating	New energy-efficient, closed-loop plating technologies		2015
	Low energy soldering equipment	New design concepts for waste energy reduction, energy reuse in soldering processes		2015
	Eco-efficient electronics assemblies	New technologies for boards, component packaging, connectors using renewable, compostable materials		2015
		New energy efficient product designs for EuP compliance		2010

Low Priority				
Issue	Challenges	R&D Needed	Notes	Target
Life Cycle Analysis	Accurate, meaningful LCA results	New industry-led initiatives to collectively agree on LCA results interpretation and liaise with policymakers		2020
Recycling and Reuse Technologies	Low cost electronics recycling	Studies of business efficiency case for recycling, cost analyses, infrastructure		2020
Eco-Design	Clean electroplating	Breakthrough replacement technologies for tin stripping		2015

Applied Nanotechnology

1. Introduction

Nanotechnology is very much the buzzword in forecasting of future technologies. Smaller, higher surface area materials are expected to have exponentially enhanced functional properties as well as enabling microscopic devices and new medical treatments, for example.

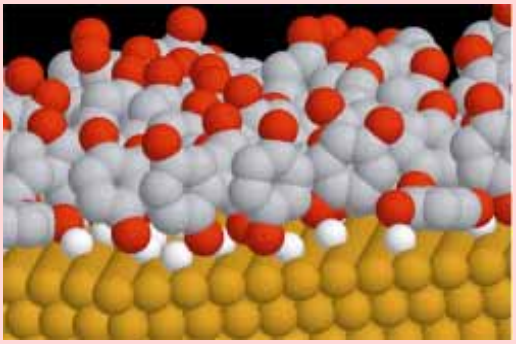
Semiconductor and wafer technologies within microelectronics already use advanced lithography techniques, for example, to produce nanostructured electronic circuitry. This is discussed in the Component Packaging section.

A totally new nanotechnological field is emerging with molecular or plastic electronics, particularly for flexible displays. This is a convergence of chemistry and microelectronic technologies using printed conductive materials to build components.

Similarly, a convergence of biology and electronics is producing new nanoscale products. Several biological lab functions can be scaled down onto a microchip to produce a ‘lab-on-a-chip’. A similar example is a microchip embedded in the body can be used for intelligent drug delivery, perhaps controlled externally by wireless.

In a quite different way, nanoparticles are attracting a lot of interest for use in materials composites to give enhanced properties. For example nanoclays can be used to enhance fire retardant properties and carbon nanotubes to enhance conductivity. Metal nanoparticles are being incorporated into conductive adhesives and there is a strong interest in researching their addition to solders.

However exciting these all sound, they face significant challenges in real use. Fabrication and manipulation techniques are in some cases embryonic. High surface energies often make nanoparticles agglomerate. Testing and reliability of electronics interconnections using biological or chemical technologies can be little more than conceptual at this stage.



2. Nano-Solders

There are at least two differing and very popular new concepts related to nanoscale solder technologies.

One is the use of nanoscale tin or solder particles in suppression of melting point, mitigating some of the thermal issues associated with higher temperature lead-free processing.

It has been known for many decades that nano-scale metal particles can depress melting point. This was discovered when extremely thin evaporated particles of metal were found to have a lower melting point than the bulk material. For example, a 50% melting point depression has been observed compared to the bulk in the case of gold.

New work using nano-calorimetry has shown significant melting point suppression happens when the particle radius approaches the sub-20 nanometer range.

iNEMI, US has recently initiated a collaborative project that attempts to apply this principle to electronics solders, based around producing and evaluating nanoparticles of tin.

Another associated idea, referred to previously, is the use of nanoparticulate additions to lead-free solders, to influence the properties such as wetting and reliability. These would be a form of composite solder. What exactly these nanoparticles would be and precisely how they would influence properties does not seem clear at this stage.

Both of these are challenged by a lack of basic knowledge of the metallurgy and microstructure of lead-free solders. There are open questions about whether such solders have any stable nanostructure or grain structure at all. Further, at room temperature, the structures are dynamic, both in the bulk and at interfaces, and ageing effects can be rapid.

Further there are commercial issues related to the viability of nanoparticulate production on the large scale and cost-effectiveness of producing such products. There are also some perceived health and safety issues with nanotechnologies generally.

Also given the very significant issues with regard to reliability and qualification of basic lead-free solders, it must surely be in the longer term that such advanced and even more complex products could be considered for mainstream adoption by the industry.

Nevertheless, enthusiasm to explore this area continues. Some initiatives have already been proposed in Europe, though none so far have achieved funding. It is expected that this will continue.

At the very least such studies will contribute significant scientific knowledge about lead-free solder micro and nanostructure.

3. Nanoscale Interconnection

Pressure to miniaturise electronics is driven both at the semiconductor level and the PCB level by consumer pressure for increased functionality, integration and portability.

At the semiconductor level the ITRS roadmap plots the course of this trend, already down to the nanometer scale. It is here that the technological limitations become apparent, for example the increase in resistivity of Cu/low k interconnection increases at small dimensions.

Nanoelectronics are thus anticipated as a future evolutionary development from microelectronics.

The European Technology Platform (ETP) for this topic is ENIAC, who in 2005 published a Strategic Research Agenda. It was proposed that work should be pursued as a part of PRINS (Pan-European Research Infrastructure for Nano-Structures).

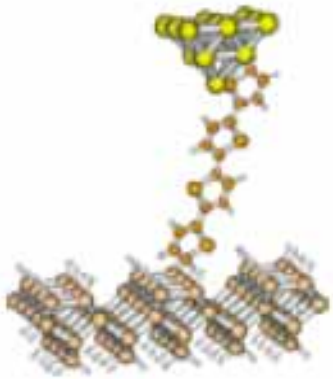
The technology status for nanoscale interconnects is largely conceptual at this stage, with some interesting new materials developments in production of nanowires, nanotubes and molecular electronics in the laboratory.

In conceiving of such new technologies, the truly small scale must be appreciated. Nanotechnology is a label often misused when actually 'very small' or actually microscale is meant.

Nanowires, for example, are almost at the atomic level. They are of dimensions of the order of 10^{-9} m, and often referred to as 1-dimensional materials. On this scale they have interesting properties not seen in bulk or 3D materials. Quantum mechanical and electrical effects are important, strength is much higher, but conductivity is lower, for example.

All of the interconnection issues described in this roadmap are relevant on the nanoscale – thermal stability, reliability, testing, integration with optical/RF interconnects etc. However, until the basic interconnect technology has been developed at all, they cannot be relevant even in the medium term.

Once the relevant nanostructures and interconnect materials are in place, then attention will need to be focussed on assembly and joining processes. At this level we are then perhaps considering molecular or chemical processes, maybe activated by photons or radicals. Concepts found in nature such as self-assembly may be useful.



4. Conductive Adhesives

Conductive adhesives are an alternative joining technology, already utilised in component packaging as, typically Ag-filled epoxy.

Research projects continue to explore the topic and undoubtedly the technology is advancing. The IMECAT project, for example, included some studies of adhesives for flexible substrates with glass and flip-chips, as well as for flip-chip on PCB.

A populist vision for many years has been replacement of standard solders by this technology but this is unlikely to be viable in the foreseeable future.

Experience of the costs and logistics of the relatively small transition to lead-free soldering technology show that such a wholesale transition would have to be very strongly incentivised.

Adhesive performance cannot yet match solders in terms of conductivity and reliability.

However, nanoparticulate technologies are likely to be developed that will push the boundaries. Significant challenges need to be overcome, for example agglomeration and stabilisation.

Reliability of the polymeric adhesives themselves in use would be limited by physical properties in relation to thermal and physical degradation, especially in harsh environments. Impact resistance and rheology could be improved. New multicomponent systems or new curing systems are needed.

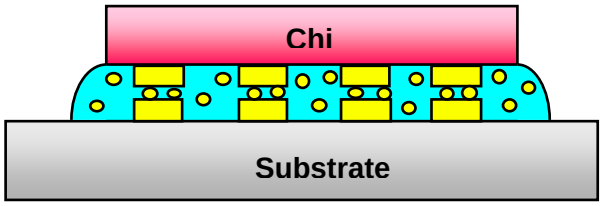
Nevertheless projects continue to explore new approaches, including, for example, the iNEMI Nano-Attach project looking at biomimectic dry adhesive systems as a replacement for SMT technology.

New use of conductive polymers may be a way forward. An example might be, for example, tin containing systems, where the tin atom is reacted into the polymer backbone. Conductive polymers are being developed for use in plastic electronics, and perhaps these concepts can be combined with adhesives.

Use and development of conductive adhesives is likely to continue, especially given the increased use of flexible substrates and more complex packaging.

Anisotropic Conductive Adhesives (ACA) were originally developed for display technologies using glass. They are now gaining widespread use, especially in Asia, though there is limited experience in Europe. They include underfill for mechanical strength. A particular advantage is in allowing very high density packaging – a 20µm pitch is 5 years is realistic.

They do have limited current capabilities and require die bumping.



5. Plastic Electronics

The concept of printable electronics has been under development for more than a decade. Some of the earlier work was printing on paper, and more recently work on textiles is developing fast.

A recent focus has been on plastic electronics for a wide variety of applications including, for example, OLED's, flexible displays, RFID, keypads and electrophoretic skin patches.

New markets for such technologies have been estimated to be worth £15 billion by 2015 and much larger beyond that.

The basic technologies use a variety of printing techniques including inkjet, screen printing and gravure methods. Materials for printing are still very much under development, but are generally based around conductive polymers, either filled with metal/carbon nanoparticles, or intrinsically conducting polymers (ICP's).

There are advantages in these technologies beyond the planar form factor. The products are much quicker and easier to make, using reasonably conventional printing processes. Further, organic semiconductors are much cheaper compared to conventional silicon semiconductors.

Much work needs to be done to develop processes to deposit and pattern (by additive printing or other methods) single and multiple organic and/or inorganic thin film layers of conductive, semiconductive, dielectric and passivation layers.

Novel (organic and inorganic) conductive, semiconductive, dielectric and passivation materials are required, compatible with processes for delivering high-resolution patterned layers on flexible substrates.

Another challenge is to develop thin films with an ability to create high-density via-holes allowing interconnection between adjacent layers of polymer and inorganic materials.

Advanced registration of multiple layers will need to be addressed, particularly for fine-line depositions over large area substrates.

Adhesion of subsequent (printed or deposited) layers without damaging existing layers is also challenging, as is improvement to planarity of intermediate and final layers of patterned materials.

Basic to the interconnection aspects is the need to deposit multiple conductive track and gap widths of 5 microns each (or less) over large areas, with demonstration of conductivity close to that of the bulk material. It is this area particularly that relates to interconnection. New metallisation technologies could be developed.

The basic principles in this development converge somewhat with developments in 3D packaging, embedded components and jetting technologies for ultrafine pitch soldering. It is thus possible to envisage a significant impact on mainstream electronics assembly. A recent UK government document has stated that "plastics electronics is poised to disrupt the world of electronic circuits".

High Priority				
Issue	Challenges	R&D Needed	Notes	Target
Nano-Solders	Cost-effective, stable lead-free nanosolders	Demonstration of melting point suppression in lead-free solders by use of nanoparticulate feed materials.		2015
		Evaluation of the effect of nanoparticulate additions on physical, processing and reliability properties of lead-free solders.		2010
Nanoscale interconnection	New materials /processes	Development of novel nanoscale materials – nanowires, nanotubes, nanostructured surfaces, nano-pillar contact bumps, molecular interconnects		2020
		Assessment of limitations of low k/Cu interconnect and develop innovative solutions – air gap, 3D		2015
Plastic electronics	Cost-effective, stable, printable interconnections	New techniques for characterisation and control of new inks and dispersions, stability to oxidation, hermeticity, ageing	Product demonstrators needed	2010
		Integration of metallisation technologies		2015

Medium Priority				
Issue	Challenges	R&D Needed	Notes	Target
Nanoscale interconnection	New materials /processes	Studies of relevant nano-interfaces and development of novel joining technologies – molecular bonding, non-thermal activation (photons, radicals)		2020
Conductive adhesives	Commercially viable large-scale technologies	Use of nanotechnology to produce and stabilise highly conductive particle dispersions		2020
		Development of new highly conductive nanoparticles for Conductive Adhesives (CA) – passivated tin, copper, polymer core	, improved impact resistance, rheology	2020
		New materials for Anisotropic Conductive Adhesives (ACA), Thermally Conductive Adhesives - self-adhesive tapes, foils		2015
		Studies of conduction, adhesion mechanisms of conductive adhesive, enhancement technologies		2015

Low Priority				
Issue	Challenges	R&D Needed	Notes	Target
Nanoscale interconnection	New materials /processes	Development of new ways to integrate electrical, RF and optical interconnects on the nanoscale		2020
Conductive adhesives	Commercially viable technologies	Studies of reliability of conductive adhesive technologies, failure mechanisms, predictive models		2020
		Development of large-scale application and curing process equipment		2020

Component Packaging

1. Introduction

Component Packaging is driven by the need for smaller, faster, cheaper electronics for both passive and active devices.

Packaging and interconnection aspects dominate the future needs for electronic systems and are key issues for many of the international technical organisations that represent the segments of industry involved in various aspects of the whole supply chain. SEMI, IMAPS, JEDEC, IPC, iNEMI, JEITA. IEEE CPMT and JISSO are all involved with setting standards and developing acceptable packaging technology.

Directions are generally determined by the Industry Roadmaps that 'push' the semiconductor market along the Moore's Law path to smaller and smaller geometries with increased functional density, in other words, more i/o pads with small dimensions. The addition of a "package" around the devices is a cost adder and a potential failure mechanism, so the eventual need is for "no package" devices incorporating Wafer level packaging features. On the other hand, 'More than Moore' opportunities are creating the need for better, more robust, package technologies to support, protect and enhance the devices in applications that are power hungry and/or require harsh ambient survivability over long periods of time.

Interconnection requirements for Passive components and electromechanical (EM) devices, connectors, relays etc., will continue to pose challenges but will tend to develop in the shadow of the needs of the active, semiconductor component. The move to embedded components will see passive elements 'packaged' into both silicon and board system substrates, either as integrated design elements or in reducing size package outline.

EM components will be 'assimilated' wherever possible by Solid State devices, but driven by the need for more robust systems. The big challenge here will be to maintain power handling, operate at higher speeds and achieve next level connection whilst continually being reduced in size.

2. System in Package (SiP)

Development of active devices is generally centred on the needs of the semiconductor industry, with directions driven by Moore's Law and the International Technology Roadmap for Semiconductors (ITRS). However some passive components, MEMS, SAW devices, crystals, piezo devices pose similar packaging challenges as do IC chips and are also being integrated into active devices at both substrate (Si) and package levels, in order to get more functionality into a smaller package.

System in Package (SiP) and System on Chip (SoC) are directly related and can be combined in any ONE Package to produce enhanced functionality and performance at optimised cost. A variety of SiP constructions are shipping in high volume today, including stacked die, planar constructions with integrated passives and stacked package modules. SiP products are now providing solutions for all high-tech electronic product designs, such as Ipods and mobile phones.

Reviewing the ITRS roadmap and other roadmaps such as IPC, iNEMI and Jisso, they all highlight the fact that future packaging is going to be much more than a chip in a package. ITRS is now essentially a roadmap for SiP applications as it has fully embraced the convergence of PCB technology and chip interconnect technology.

SiP is forecast to be a combination of Wafer level Packaging (WLP) and direct chip attach (DCA) to system board and/or application. It is heavily focussed on chip to board technologies, including bumping, flip chip and micro-nano interconnections as well as automation. These are also key future technologies related to WLP which, like 'chip mount' technology (CMT) is pushing for new processes, new machinery, new materials and new ideas to be developed to match expectations.

SiP structures need to be carefully designed to overcome the requirement for complex signal-integrity analysis. New software tools are emerging that will assist the silicon designers and system architects to design and test chip-to-chip interconnections that support signal rates beyond 25Gbps, using open-source, licensable IP design components, which include patented IC packaging solutions, channel layout and electrical connectors. However such software usage is likely to add significantly to overall packaging costs. Additionally, many of the parameters that need modelling are relatively unknown. There is a need for a database of critical dimension values, Dielectric constants, CTE matches and other mixed material properties.

Chip and package co-design are critical to success, some of the tools are out there but there is no one packaging centre that can provide emerging technology solutions and quick turn support to get prototype – to pre-production volumes into the market. A Centre of Excellence, equipped with the right (state of the art) equipment is needed. There is sufficient support in Academia and Industry research, as well as technical support centres such as NPL, Tyndall, Fraunhofer and IMEC to qualify and quantify the necessary technologies, however a focussed group needs to be set up that can utilise and develop the technologies to support successful implementation.

3. 3D Interconnects

Multichip packages, such as SiP, Package on Package (PoP) and even Package in Package (PiP) solutions take advantage of the third dimension to interconnect multiple IC die. All have a common objective in that they create performance-enhancing opportunity while limiting cost.

The JEDEC-standard PoP technology has a fully overmolded top package and capped bottom package with a four-layer substrate (see below).

Here the key objective is defining chip type interface standards that can enable .interconnect stacking protocol for reduced package wiring density and improved electrical performance.

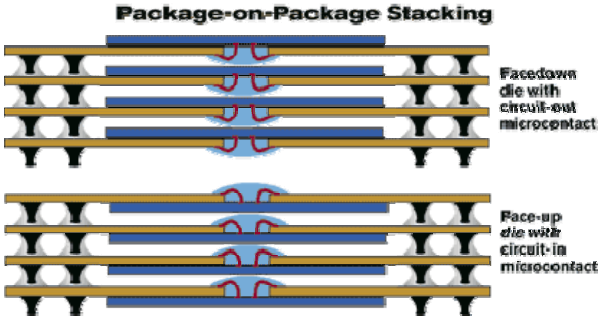
By thinning, stacking and connecting chips, 3-D is a way to greatly increase functionality, a goal common to many packaging technologies such as system-in-package (SiP). But 3-D processes require more front-end type processing, as does WLP. Recent IBM research for 3-D integration has concluded that high pattern density designs of copper interconnects exhibit the best bonding yield. In addition, under optimized bonding conditions, a strongly bonded interface with precise alignment and excellent electrical connectivity can be achieved.

This key advanced package technology will inevitably be mainly chip stacking. Processes will require modified traditional back-end packaging methods, like pyramid chip stacking with wire bond. Others will utilise chip-to-chip stacking that is similar to multilayer PCB construction, but dimensionally much smaller. This will require a process that thins the wafers, forms and fills microvias, aligns and bonds the stack. Additionally the bottom layer will need to be bumped to make a 3-D flip-chip, at wafer level (WLP). Packaging requirements already need more wafer-level services as front end and back end converge.

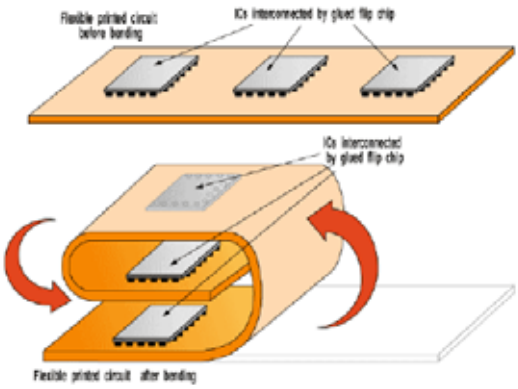
The needs of equipment for all new and emerging applications will put demands upon all levels of interconnection between the semiconductor chips and the complete system interfaces. The aspects that will need research and qualification will be issues for system designers, system integrators, PCB designers and manufacturers right down through chip packaging to chip designers and manufacturers. In addition, the constraints imposed upon materials and equipment providers to meet the needs of 'next generation' interconnection will pose further demands on the metrics relating to process control, environmental compatibility and system performance.

A relevant example is the need to use and process solders with different melting points for multi-step joining.

Stacked die/package arrangements give the advantage of assembling die that have



been tested and burned in as packaged devices. Tessera (USA) has developed a new contact for its stackable package to reduce height. (see below).



Here, microcontacts are designed to enable package-on-package stacks with board connections.

Folded flexible Circuitry is envisaged as a key capability in 3D packaging. 3D Flex packages excel in miniaturization, lightness and durability, but also provide configurability for multi-chip modules. Flex packages include CSPs, Chip-on-Flex, TAB, Tape Carrier Packages, microBGAs, TapeBGAs, FlexBGAs and folded arrays.

Flex circuits have been in existence for over 20 years, yet have been used in relatively few applications. Increasing pressures to miniaturize (thus impacting design space) and market forces driving high quality and low-cost products are two reasons why use of this technology will increase in the coming years.

Flex is the ultimate high density interconnect (HDI) with thin conductors and dielectrics that provide maximum density with trace widths below 12 µm. High density, electronic stability, material flexibility, extreme thinness, and exceptional thermal resistance are needed for packaging.

VALTRONIC uses the folded concept as shown below to combine logic, memory, and passive components into a single SiP for use in hearing aids and pacemakers.

However a number of areas need to be developed for future technology matching, such as Design tools and reliability data for Vias, Holes, Bending radii, edge effects, Pad stacks and track routing. Also there is a need to embed parts on internal layers of the stack to fully integrate the system functionality.

A folded-stack CSP in use today, uses TESSERA's patented 3D mZ foldover ball stack concept for up to eight DRAM, SRAM, or flash memory chips to be stacked into a multichip assembly. It uses a flat, flexible polyimide tape attached to a chip die and then folded over for interconnecting the next stacked die on top. The optimisation of packaging and interconnects is a critical design process and reliability aspects are in need of evaluation.

The technologies for materials to achieve even smaller dimensions and higher densities need to be developed. Some research is underway at IMEC to demonstrate sputter deposition processes to achieve fine resolution metallisation and tracks to enable improved 3D wafer level packaging and support integrated passive devices.

Yet there are still significant technical challenges for SiP processing, such as aspects of Wafer thinning, reliability effects of heat paths at the system level as SiPs get denser and smaller. It is envisaged that several generations of SiPs with higher integration levels will be developed as determined by the iNEMI SiP roadmap which calls for future placement equipment that can handle die placements from wafer formats with at least 15-µm accuracy at less than $0.005 per placement. Industry can't meet such a goal with current assembly equipment.

4. Interconnect Spacing

Besides the trend towards higher integration density, there is also a demand for more functionality and increased performance. Mainstream technology already has physical and technological limitations, which have a severe impact on system characteristics. Added device content, will also increase chip area and push for reduction in interconnect spacing.

The performance, multifunctionality and reliability of microelectronic systems are now becoming limited mainly by the wiring between the subsystems and will lead to a critical performance bottle-neck for future IC generations as detailed in the ITRS.

Here the reduction in device geometry and die size is the driver for reduced size packages and future CSP and Fine pitch FBGA will be down to 0.15um pitch. Matching this package pitch at the next level of interconnection will pose very difficult engineering aspects for all materials and technologies. New process technologies are needed to realize narrower traces and spacing.

Increased use of tin based soldering compounds may increase the propensity for tin whiskers and, as detailed in other sections of this report, work is required to develop design rules and new techniques for mitigate the risk of tin and other material whiskering. The greatest risk is from pure tin, though in most cases there are amounts of other elements such as Ag, Cu etc. Several percent of these elements will decrease whisker propensity close to zero.

Matching the device spacing on both substrates for packages and on system boards will require technology and equipment development to achieve a reliable product. A process will be required that has ways of preventing Copper (Cu) dissolution during processing devices with thinner tracks.
These processes will inevitably only work with new materials that can be selected to increase reliability by avoiding Cu dissolution, electro-migration and other intermetallic effects.

With fine pitch geometries power “crowding” and performance limitations will need to be understood. Current density of the order of 10^4 A/cm^2 is a limiting parameter for Power handling.

Interconnection and packaging of low power circuits generates a different set of challenges. Innovative solutions are needed to overcome detrimental current crowding effects in the power management and control grid structure of gate array devices. Such work will include not only the on-chip line spacing and structure but also the design of the i/o and interface connections.

5. Vertical Interconnects

Classical packaging and interconnect technology is developed and engineered for X-Y dimension systems. Future packaging technology is becoming more and more aware of the issues affecting the third 'Z' dimension of the interconnect.

3-D integration concepts can be classified into three categories:

- Stacking of packages
- Stacking of ICs
- Vertical System Integration

These methodologies are also required by the optoelectronic, photonic, sensor and MEMS manufacturers. Development of vertical interconnection technologies provides an ideal way of increasing the packaging density of devices such as camera chips and media sensing, where the sensitive detection surfaces can be isolated away from the need for next level interconnection.

Vertical interconnection at the chip level is the current goal of process development work for sensor and WLP devices. The DRIE type processes, such as the BOSCH patented method, are being utilised in the MEMS manufacturing area but have limitations in packaging above chip level.

Similarly, development of "front end" type equipment and technology will be required to support implementation of vertical plane direct bonding techniques.
Processes of printing, sintering, electroplating, electroless deposition, physical and chemical vapour deposition (PVD, CVD) have to be developed.

At higher levels of packaging vertical interconnects will be employed for board and device packaging that will require development of new materials and fabrication processes.

Transient Liquid Phase Sintering (TLPS) fabrication is an emerging soldering technique where the solder is never completely liquid. This could offer several important advantages in joining processes as well as increased flexibility in design and processing. It allows a good vertical interconnection and a multi-stage, step wise soldering process. It is also possible to be used in applications where fusion to the base metal has to be avoided

The development of nano component technologies will also be required to support advancement of package technologies utilising pin insertion by press-to-fit or insert and contact techniques.

6. Embedded Components

Conventional Chip integration concepts are based on embedded technologies, but there are serious disadvantages as a result. Large chip areas cause yield problems and the chip partition with the highest complexity determines the processing technology. For chip packaging similar embedded component now aspects need to be considered.

3D system integration is one way to overcome some of the drawbacks, reduce volume, weight and power consumption of next generation components. Embedding components into the packaging and/or the system substrates has the capability to add even higher levels of integration into the overall system.

Embedding the chip devices, either into PCB or Ceramic substrates or into the package materials directly will involve new technologies for component processing, assembly, interconnection and test. The key aspect for embedded ICs will be preparation methodology for Wafer thinning as this will have a range of associated issues that may affect device functionality. Vertical interconnects are potentially a key enabling technology for this process.

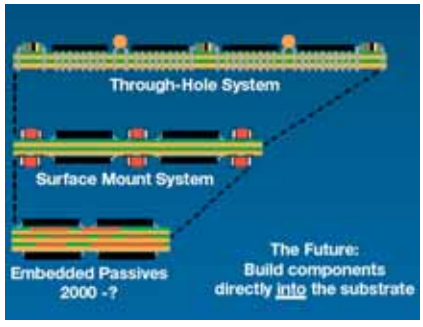
Development of both placing and joining techniques for insertion of components will also be required. The size, number of interconnects and the accuracy of alignment are crucial aspects. A number of other issues will need to be resolved such as effect of process upon frequency of operation, parasitic effects of surrounding materials, stress, strains of assembly processes, use of interposer materials and sealing processes and thermal matching.

In addition to determining a viable interconnect ion methodology it is envisaged that new techniques for adjustment of embedded functions with capacitance trimming and inductance matching will be required.

Realisation of comprehensive design rules for embedded and mixed technologies will be a significant challenge. The aspects to be considered will cover may features including: Bond pad vs. Die pad geometries, track routing, integral bond pads and finger shapes, interconnect process of bond wires or direct chip attach

Embedding sensor components into packages is now an emerging aspect of packaging research. In the USA, Georgia Tech is involved in a number of projects incorporating SMT sensors into packages. ‘Health Monitoring’ sensors (HUMMs) are being developed in Europe as reported by the PATENTDfMM project. Here integrated thin film sensors are incorporated as part of the system package to measure and monitor operational aspects of the devices.

It is expected that these technologies will be developed and applied to ‘wearable’ electronics systems which will be eventually considered for commercialisation.



7. Thermal Management

Heat generated by electronic devices and circuitry must be dissipated to improve reliability and prevent premature failure. Techniques for heat dissipation can include heat inks and fans for air cooling, and other forms of computer cooling such as liquid cooling. The component package now has to provide significant thermal management capability and future demands are unlikely to be met unless some novel processes can be developed.

The packaging community has been providing thermally enhanced devices for many years but as devices geometries shrink, the internal junction thermodynamics create more heat and increased functionality requires more power, which in turn generates a higher thermal load. Additionally, self-heating induced by vias and metal/Si contacts in VLSI circuits is undoubtedly one of the most important reliability issues for microelectronic integrated circuits.

The ITRS roadmap is also seeing an increase in operating ambient from 45 to 55 ^{o}C and harsh environments going up to 200 ^{o}C in the next 10 years.

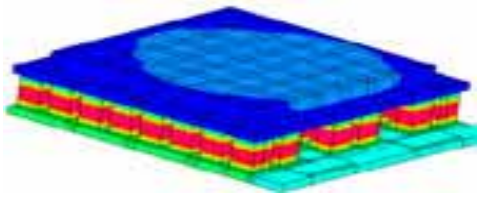
A variety of tools to evaluate and model thermal effects are available from companies such as FLOWMERICS however the necessary thermodynamic data is unlikely to be available for modelling some of the new devices and new packaging technologies being determined. Dissemination of information about new thermal management, design and test tools has to be supported by future projects. Thermal management has to be part of the design process of the device itself, its package and the system.

Coplanarity of devices is a major issue for assembly processes and is compounded in a number of new package technologies such as BGA and CSP by the need for thermal management processes. Ensuring component coplanarity during reflow is a major problem in search of a comprehensive solution. Additionally measurement and prediction of Warpage of BGA type components is considered a need in determining interconnect reliability.

Research into new materials and technology for heat dissipation is on the agenda of many research and Academic organisations in USA and Asia (according to IMAPS) however it is aimed at the system and/or the end product rather than the component packaging industry.

Development of new principles to collect and remove heat, like cooling by condensation, use of heat-pipes, heat engines and pyro-electric materials are required. In addition the thermal dynamic behaviour of new organic materials, such as organic polymers, graphite and diamond, needs to be investigated.

Advanced cooling techniques with the application of new materials have to be considered essential for advanced component packaging. This may require fundamental changes in package design and already the consideration is being given to the application of micro-fluidics for thermal management in high reliability applications.



Component Packaging

High Priority				
Issue	Challenges	R&D Needed	Notes	Target
System in Package (SiP)	Sub-Systems linking	Interconnect linking between components	Methodology for design and implementation with verification of tools to achieve accuracy	2010
		Data for modelling interconnections	Generation of Device Parasitics database	2010
3D Interconnects	New/improved 3D packaging methods and approaches	Stacked chip interconnect processing aspects including through via and wafer bonding	Feature sizes of +/- 1 micron and alignment tolerances. vias ratio 20:1 – 100:1	2010
		System in Package (SiP) assembly process qualification		2015
		Package on Package (PoP) assembly process qualification		2015
		Folded flexible circuitry - bending radii material properties		2015
	Better reliability	Reliability data for copper-to-copper bonding - surface condition, development of 'clean' processes.		2010
Interconnect spacing	Lower power density	Interconnection and packaging of low power circuits		2015
Vertical interconnects	New fabrication concepts	Development of direct bonding techniques	E.g. printing, electroplating, vapour deposition	2015
Embedded components	Better processing	Design rules for embedded and mixed technologies.	CTE data, parasitics	2010
Thermal management	New tools	Dissemination of information about new thermal management, design and test tools	Develop SME involvement	2010
		Development of new principles, like collect & remove heat; cooling by condensation; heat-pipes	Incorporate tools into commercial software	2015
	Advanced materials	Advanced cooling techniques with the application of new materials	Database technologies vs materials vs applications	2010
		Application of microfluidics for thermal management		2015
	Stable coplanarity	Measurement and prediction of Warpage of BGA type components	Dynamic stress measurement methodology	2010
		Ensuring component coplanarity during reflow	Ibidem	2010

Medium Priority				
Issue	Challenges	R&D Needed	Notes	Target
3D Interconnects	New/improved 3D packaging methods and approaches	New 3DMID technologies		2015
	Improved power management	Current crowding analysis tools		2010
		Power dissipation methods		2015
	Better reliability	Thermal Management modelling		2015
		Intermetallic effects of small scale joints		2010
Interconnect spacing	Cu dissolution with thinner tracks	New materials to increase reliability by avoiding Cu dissolution, electro-migration, etc		2010
	Finer Pitch	New process technologies to realize narrower traces and spacing		2015
Vertical interconnects	New fabrication concepts	New materials and processes, e.g. Transient Liquid Phase Sintering,		2010
		Pin insertion by press-to-fit or insert & contact techniques		2010
Embedded components	Better processing	Wafer thinning to prepare embedded ICs		2010
		Placing and joining techniques for embedded components		2015
		Adjustment techniques for embedded passives		2010

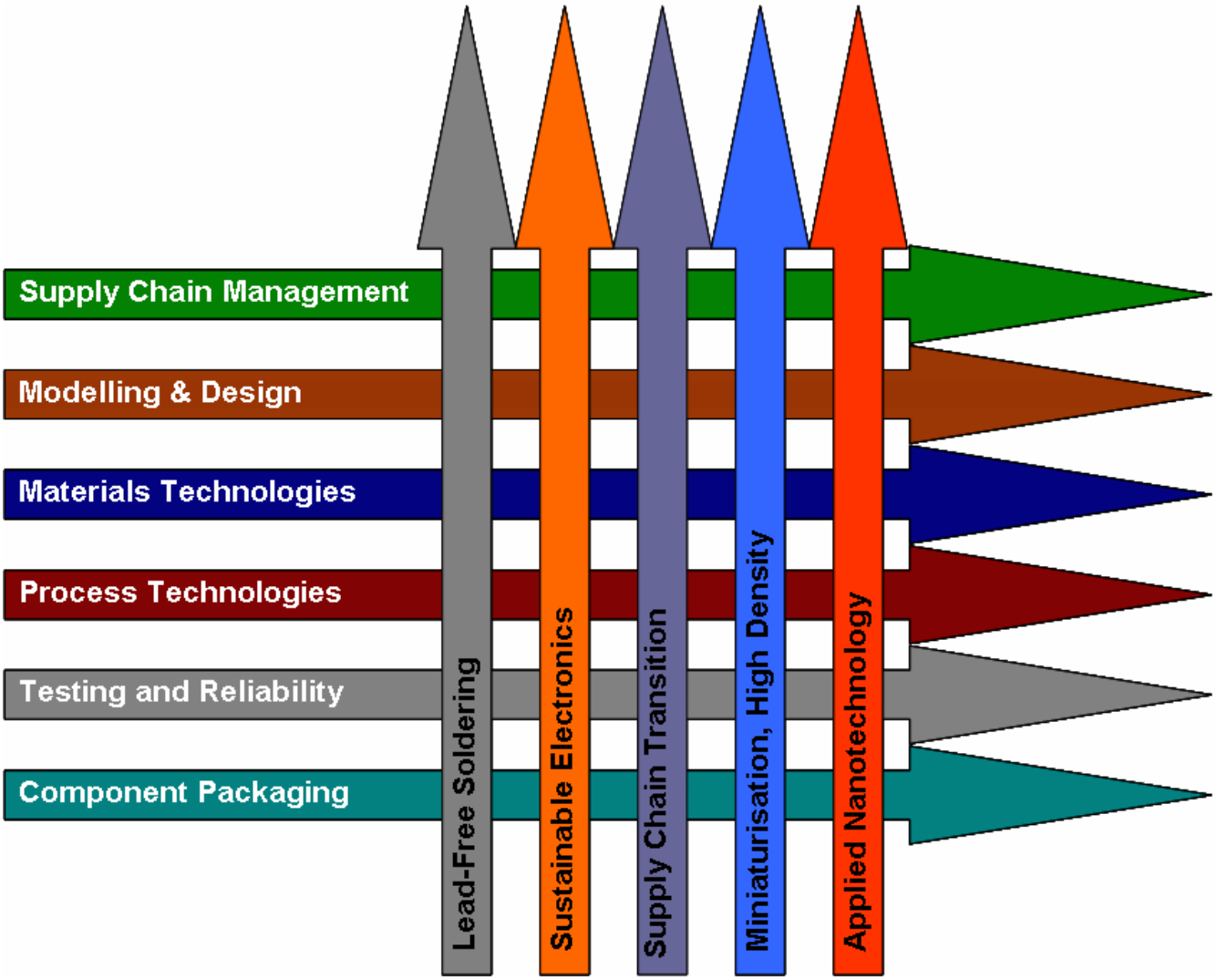
ELFNET Roadmap

European Electronics Interconnection

ANNEX – Interconnection Drivers and Trends

INTERCONNECTION DRIVERS

The diagram below summarises the key technology domains in electronics interconnection and the cross-cutting drivers currently affecting the direction of technology development, as discussed in the ELFNET Roadmap.



INTERCONNECTION TRENDS

The following table summarises responses from 5 typical European industry leaders in key use sectors, forecasting changes in testing, design specifications and process techniques to 2009. This can be compared to similar data elsewhere, notably the US IPC Roadmap.

European Electronics Interconnection Trends to 2009

Demand	Mobile Products		Prototype Research for Consumer & Mobile Products		Consumer & Automotive Products		High End Electronics: Aerospace, Medical, Telecom		Automotive (Electronic control units, sensors)	
	Present	2009	Present	2009	Present	2009	Present	2009	Present	2009
Reliability										
Life time cycles	-55/+125ºC 1000 cycles	-55/+125ºC 1000 cycles	-55/+125 ºC 1000 cycles	-55/+125 ºC 1000 cycles	Consumer: 0/100 ºC 2500 cycles Automotive: -40/+125ºC 2500 cycles	Consumer: 0/100ºC 2500 cycles Automotive: -40/+125ºC 2500 cycles	-55/+125ºC 1% 500 cycles	-55/+125ºC 1% 500 cycles with adapted dwell time	-40/+125ºC 1000 cycles	-40/+155ºC 2000 cycles
Vibration			3-20g 10-1000 Hz 12-30 hr	3-20g 10-1000 Hz 12-30 hr			Reson. Freq. 30g X-Z axis 10 hr	Reson. Freq. 30g X-Z axis 10 hr	3-20g 10-1000 Hz 12-30 hr	3-20g 10-1000 Hz 12-30 hr
Shock	85/85%H 1000 hrs	85/85%H 1000 hrs	85/85%H 1000 hrs Thermal storage 150ºC	85/85%H 1000 hrs Thermal storage 150ºC	JEDEC JESD 22B111:30x	JEDEC JESD 22B111:30x (to 50x)	11ms 100g X-Z axis 25 shocks	11ms 100g X-Z axis 25 shocks		
Substrates										
FR4 thickness	0.6-1.2mm HDI	0.4-0.8mm	2mm 100x100mm	2mm 100x100mm	0.6-1.6mm	0.6-1.6mm	1.6-2.5 mm 233x160mm High perform.	1.6-2.5 mm 233x160mm High perform.	e.g. 1.6mm 180x200mm	e.g. 1.6mm 180x200mm
Flex	PI, single, double, multi	PI, single, double, multi, rigid-flex		Desirable	PI	PI, 0.1mm FR4/PEN foil				
Ceramic					Automotive: Al2O3, LTCC	Automotive: Al2O3, LTCC				
Line/Space	100µm / 100µm	50µm/ 50µm	100µm / 100µm	≤50µm/ 50µm	100µm / 100µm	75µm/ 75µm	100µm / 100µm	75µm/ 75µm	100µm / 100µm	75µm/75µm (50µm/50µm)
Min dam sold. mask	75µm	50(75)µm			150µm	75µm	100µm	75µm	200µm	150µm
Number of Cu layers	4-8	6-12			2-8	2-8	10-16 (daughter)	12-20 (daughter)	2-6	2-8
µvias, µvia in pad, buried vias..	µvias, µvia in pad, buried vias	µvias, µvia in pad, buried, stacked vias			TH via: 0.2mm BuildUpFoil: 25 µm	TH via: 0.2mm BuildUpFoil: 25 µm	µvias (2+x+2), buried vias	µvias (4+x+4), µvia in pad, buried vias	100 µm via, µvia (1+x+1)	75 µm via, buried vias, µvias (2+x+2)
Board finish	OSP, OSP+ENIG, ENIG/Imm. Sn, Imm Ag	OSP, OSP+ENIG, ENIG/Imm. Sn, Imm Ag			NiAu, CuOSP	CuOSP, Imm Sn, ImmAg	HASL (SnPb), NiAu, Sn	Sn, Ag, NiAu	NiAu, Sn	NiAu, Sn

Electronic Components										
Min. pitch	0.5 mm	0.3 mm	400 µm	200 µm	0.5 mm	0.4 mm	0.5 mm	0.5 mm	0.4 mm	0.4 mm
Min pad size (C0603)	0201: 300 x 250 µm	01005: 200 x 200 µm	0201 components	01005 components	0201: 0.5 x 0.5 mm	01005: 200 x 200 µm	0.85 x 0.95 mm	0.85 x 0.95 mm	0.65 x 1.1 mm	0.5 x 0.5 mm
Min pad size (D^2 Pack)		2.5 x 2.5 mm – 10 x 10 mm			3 x 3mm	3 x 3mm	10.5 x 8mm	10.5 x 8mm	3 x 3mm	3 x 3mm
Min chip format	0201	01005			0201	01005	0402	0402	0402	0201
BGA 1/1.27mm – size	32 x 32 mm	32 x 32 mm			32 x 32 mm	32 x 32 mm	Ceramic & plastic 45 x 45 mm	Ceramic & plastic 45 x 45 mm	32 x 32 mm	32 x 32 mm
MicroBGA 0.8/0.65 mm	15 x 15 mm I/O 350	15 x 15 mm I/O 500			15 x 15 mm I/O 300 0.5 mm pi	15 x 15 mm I/O 300 0.5 mm pi	I/O ~300	I/O ~300		11 x 11 mm I/O <80 0.8 mm pi
CSP <= 0.5 mm	2.5 x 2.5 mm – 15 x 15 mm	2.5 x 2.5 mm – 15 x 15 mm			2.5 x 2.5 mm 0.5 mm pi	2.5 x 2.5 mm 0.4 mm pi	I/O 256	I/O 256		<12 x 12 mm I/O <330 0.5 mm pi
QFN – exposed pad		5 x 5 mm 0.4 mm pi				4 x 4 mm 0.4 mm pi		10 x 10 mm 0.5 mm pi		6 x 6 mm I/O <50 0.5 mm pi
FC									4 x 5 mm I/O 22 0.32 mm pi	11 x 11 mm I/O 530 0.35 mm pi
Process technologies										
Solder deposition	Stencil printing	Stencil printing	Stencil printing	Stencil printing	Stencil printing	Stencil printing	Stencil printing	Stencil printing	Stencil printing	Stencil printing
Stencil thickness	100-150 µm	50-100 µm stepped	75-150 µm	50 µm	125 / 100 µm	125 / 100 µm	150 µm, staggered	150 µm, 100 µm staggered	150 µm	150 / 100 µm
Solder paste	No clean, Type 3-4	No clean, Type 5-6	Type 4	Type 6	Type 3-4	Type 6	No clean (but cleanable) Type 3	No clean (but cleanable) Type 5	Type 3	Type 5
Solder alloy	SnPb, SAC	SAC	SnPb, Pb-free (SAC & SnCu)	SnPb, Pb-free (SAC & SnCu)	SAC	SAC+?	SnPbAg (2%)	SnPbAg (2%), SAC	SnPb	SAC
Soldering	Reflow	Reflow	Reflow	Reflow	Reflow	Reflow	Reflow, Wave, Manual	Reflow, Wave, Manual	Reflow	Reflow
Testing technology	X-Ray, AOI	X-Ray, AOI	X-Ray, SEM	X-Ray, SEM	X-Ray, AOI, ICT	X-Ray, AOI, ICT	X-Ray, AOI, bound. scan, probe, in situ	X-Ray, AOI, bound. scan, probe, in situ	X-Ray, AOI	X-Ray, AOI
Conformal coating	No	No			Not standard	Not standard	Spray (Man, robot)	Spray (Man, robot)	Not standard	Not standard

Wafer Bumping										
Max wafer dia.			200 mm	200 mm	6 inch	12 inch			200 mm	200 mm
Solder paste			Type 6	Type 8-9	Type 6	Type 8			Type 6	Type 6
Solder deposition			Stencil printing	Stencil printing	Printing	Print/?Jetting			Stencil printing	Stencil printing
Soldering			Reflow		Reflow				Reflow	
Min pitch			100–80 µm peripheral 150 µm area	60 µm peripheral	380 µm	60 µm			320 µm	200 µm
Min stencil opening			50 x 125 µm	35 x 80 µm	190 µm	40 µm			220 x 300 µm	130 x 260 µm
Max stencil opening					3 x 3 mm	3 x 3 mm			3 x 3 mm	3 x 3 mm
Min wafer thickness			300 µm	150-200 µm	400 µm	200 µm			525 µm	200 µm (150 µm)
Stencil thickness				20 µm						50-100 µm
Manufacturing method			Laser-cut, Electroformed	Laser-cut, Electroformed					Laser-cut	Laser-cut, Electroformed
Number of bumps									~50,000	~150,000